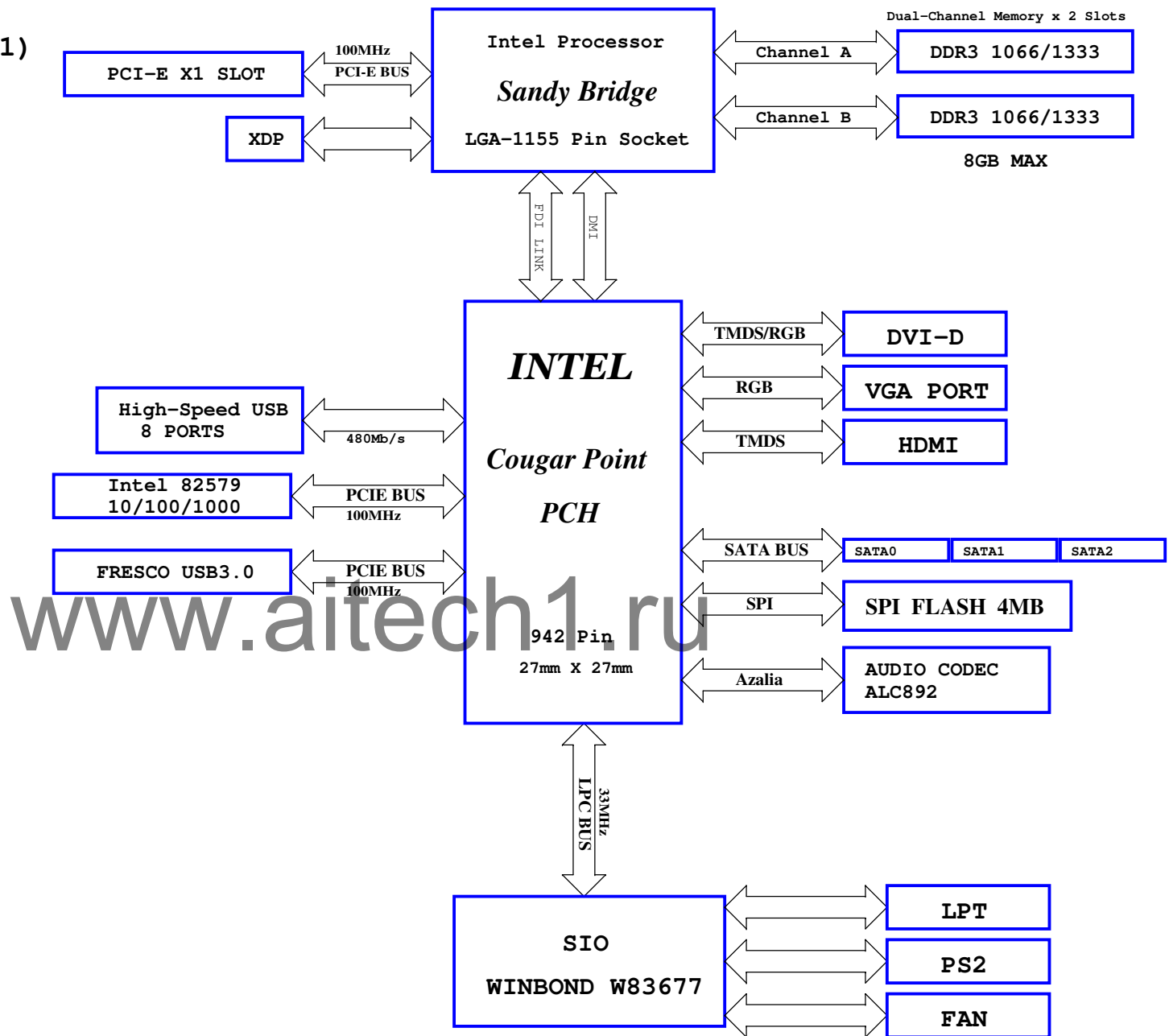


# IPX61-DL

Revision: 1.00-A01 (2010/09/21)

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02	CHANGE HISTORY - 1
03	CHANGE HISTORY - 2
04	CLOCKS DISTRIBUTION
05	SIGNAL & RESET MAP
06	POWER FLOW
07	POWER DISTRIBUTION
08	POWER SEQUENCE
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15	PLTRST_CPU#
16~18	DDR3 & TERMINATION
19	SMBUS
20~28	INTEL_PCH(1~9)
29	PCH_DPWROK & SUS_ACK#
30	VGA PORT
31	PRINT_PORT
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34	HDMI CONNECTOR
35	MINI_PCI-E_CARD
36	SATA CONNECTOR
37	P/S2&USB
39	INTEL 82579 LAN CONTROLLER
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42	RJ45+USB 3.0 CONNECTOR1
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50~51	SUPER I/O -WINBOND W83677HG-I
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55	SM BUS & SPI ROM & BIOS CONF
56	FRONT PANEL & LPC DEBUG
57	RTC / CMOS / SPKR/ SCREW
58	CPU XDP DEBUG CONNECTOR
60	ATX POWER 24P CONNECTOR
61	+3VA & +3VSB & +5VSB
62	+1P5V_DUAL
63	+VTT_DDR & +1P5V_DUAL_EN
66	+5V_DUAL & +5V_DUAL_USB_B/F
67	+1P05_PCH & +1P8V_SFR
68	+1V_DUAL
69	+3P3V_LAN & +3P3V_ME & +1P05_ME
70	+1P05V_CPUIO CONTROLLER
71	+1P05V_CPUIO DRIVER
72	VCORE CONTROLLER
73~74	VCORE DRIVER 1-2
75	+V_AXG DRIVER
76	VCORE CAP & OV circuit
77	INTERNAL SPEAKER



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title: **BLOCK DIAGRAM**

Pegatron Corp. Engineer: **KJ Chang**

Size A3	Project Name <b>IPX61-DL</b>	Rev 1.00
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Date: Wednesday, September 29, 2010 Sheet 1 of 74

## Schematics Change History

[illegible]

### CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

I = Installed Part.

NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

## Schematics Change History

[illegible]

**CAD Note:**

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

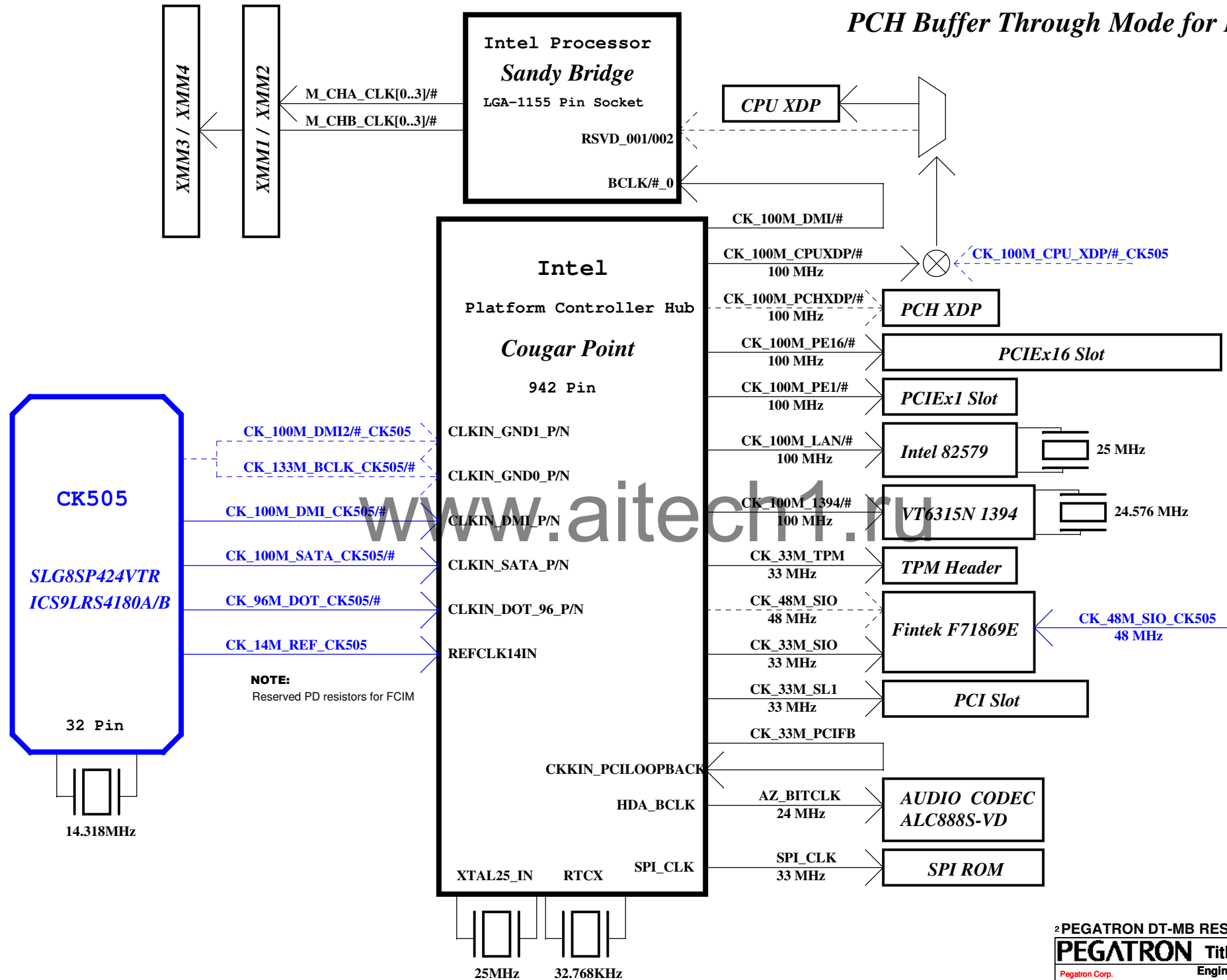
I = Installed Part.

NI = Not Installed Part.

PROTO = PROTO Phase Only.

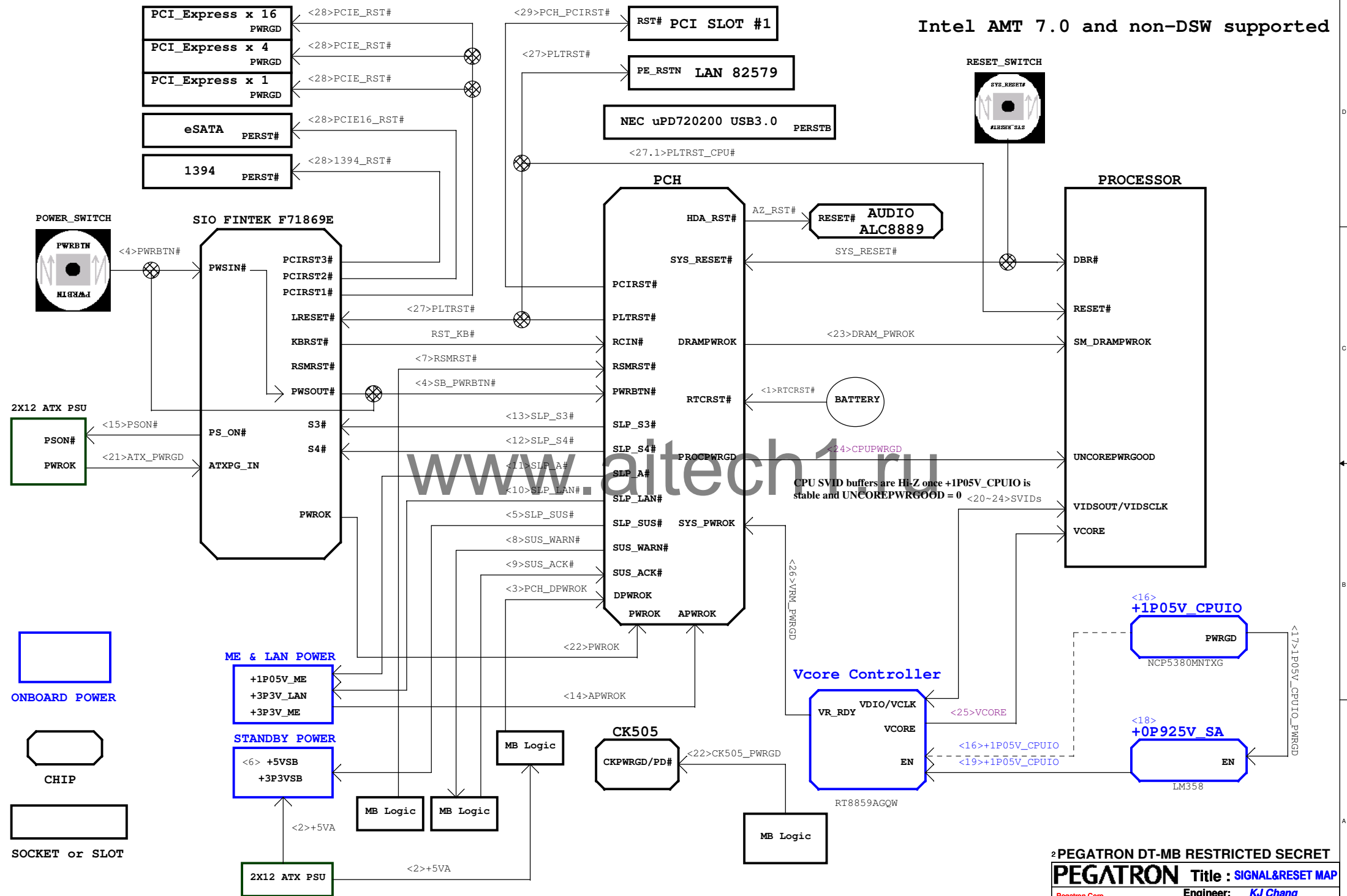
VP = Virtual Part.

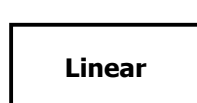
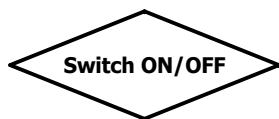
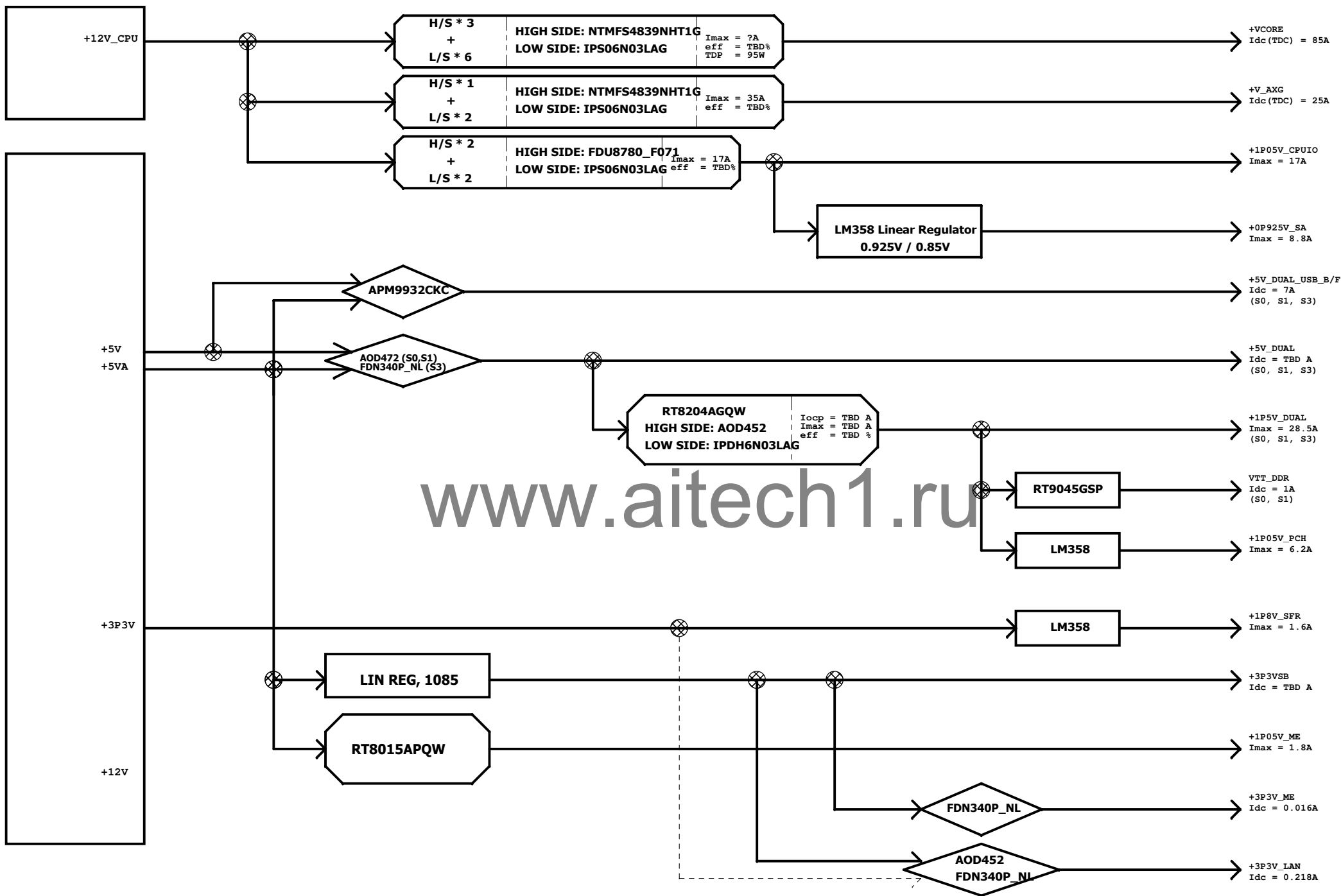
# PCH Buffer Through Mode for Pre-Silicon





Intel AMT 7.0 and non-DSW supported





Note: lxx/loo  
means  
ltdc/lmax

<b>CPU Sandy Bridge</b>	
+VCORE	-> 85A (TDC) - 95W
+1P05V_CPUIO	-> 17A (Imax) - W
+0P925V_SA	-> 8.8A (Imax) - W
+V_AXG	-> 25A (TDC) - W

<b>CLOCK GEN</b>	
+3P3V	-> 125mA - W

<b>PCH</b>	
+1P05V_PCH	-> 5.831A - W
+1P05V_CPUIO	-> 0.043A - W
+1P8V_SFR	-> 0.16A - W
+3P3V	-> 0.267A - W
+3P3VSB	-> 0.107A - W
+1P05V_ME	-> 1.01A - W
+3P3V_ME	-> 0.02A - W
+3P3VA	-> 0.002A - W
+BATT	RTC (G3) -> 6uA - 0.0198mW

<b>DDR2 DIMM (4) &amp; Termination</b>	
+1P5V_DAUL	VDD (S0, S1, S3) -> 7.5 A - 11.25W
+VTT_DDR (0.75V)	SM VTT (S0, S1) -> 1A - 0.75W

<b>PCI Express x 1</b>	
+12V	-> 0.5A - 6W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE -> 20mA - 66mW

<b>PCI Express x 16</b>	
+12V	-> 4.4A - 52.8W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE -> 20mA - 66mW

<b>PCI SLOTS</b>	
+12V	-> 0.5A - 6W
-12V	-> 0.1A - 1.2W
+5V	-> 5.0A - 25W
+3P3V	-> 7.6A - 25.08W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE -> 20mA - 66mW

<b>INTEL 82579</b>	
+3P3V_LAN	-> mA - 720mW

<b>SIO Fintek F71869E</b>	
+3P3V	-> 35mA - mW

<b>ALC888S-VD Codec</b>	
+3P3V	-> mA - mW

<b>NEC uPD720200 USB3.0</b>	
+3P3V	-> 15mA - W
+1P05V_USB	-> mA - W

<b>USB 14 PORTS</b>	
+5V_DUAL_B/F	(S0, S1) -> 7A - 35W

<b>1394A VT6315N</b>	
+3P3V	-> mA - W

<b>HDMI</b>	
+5V	-> mA - mW
	-> mA - mW

<b>DVI</b>	
+5V	-> mA - mW
	-> mA - mW

<b>DP</b>	
+3P3V	-> mA - mW
	-> mA - mW

<b>FANS</b>	
+12V	-> 1.2A - 14.4W

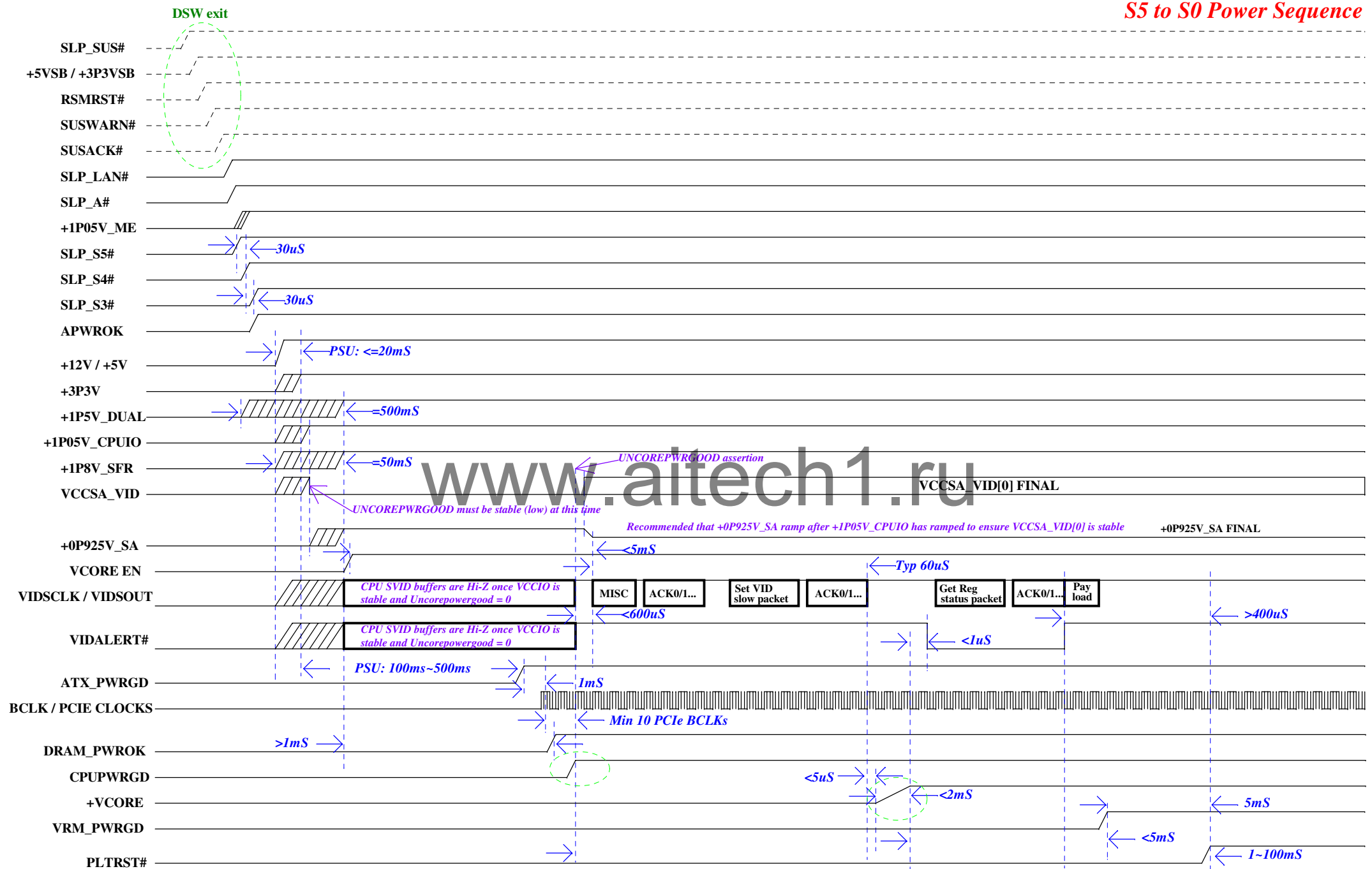
  

<b>PS2 KB/MS</b>	
+5V_DUAL	(S0, S1) -> 0.345A - 1.73W (S3) -> 2mA - 10mW

<b>SPI</b>	
+3P3V_ME	-> 30mA - 99mW

# S5 to S0 Power Sequence

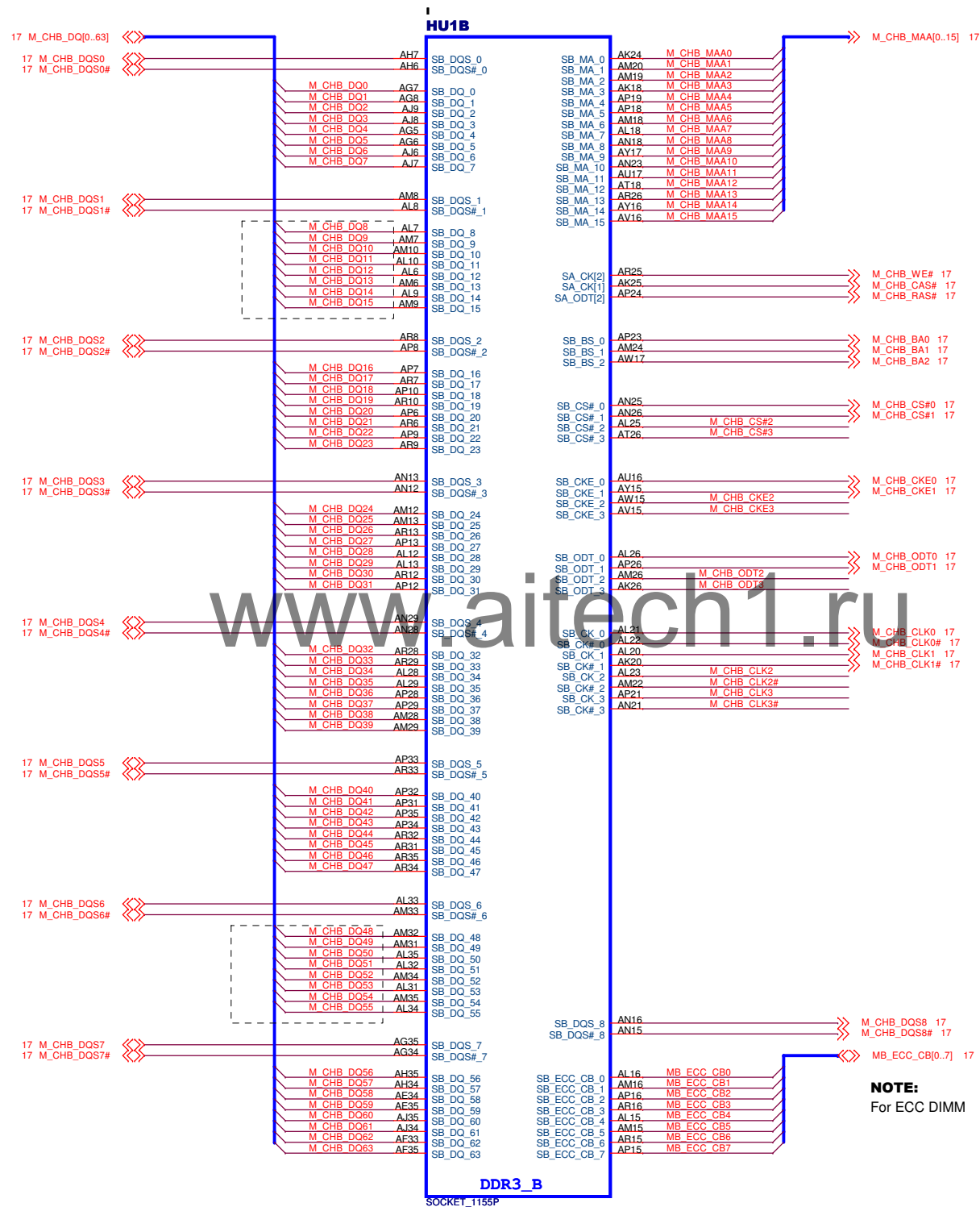


2 PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : POWER SEQUENCE  
Pegatron Corp. Engineer: KJ Chang

Size	Project Name	Rev
A3	IPX61-DL	1.00
Date: Wednesday, September 29, 2010	Sheet 8 of 74	





**NOTE:**  
For ECC DIMM

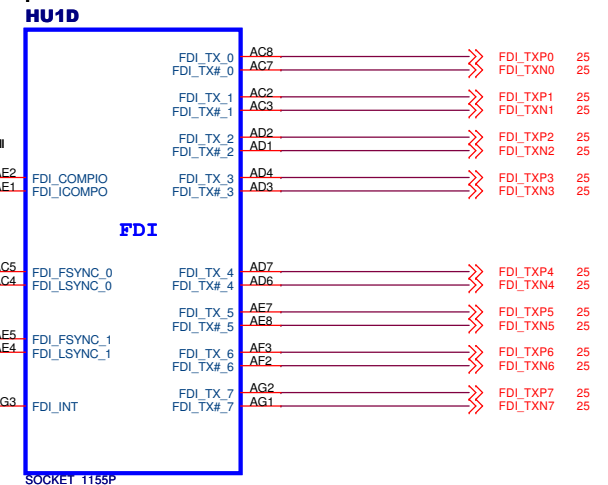
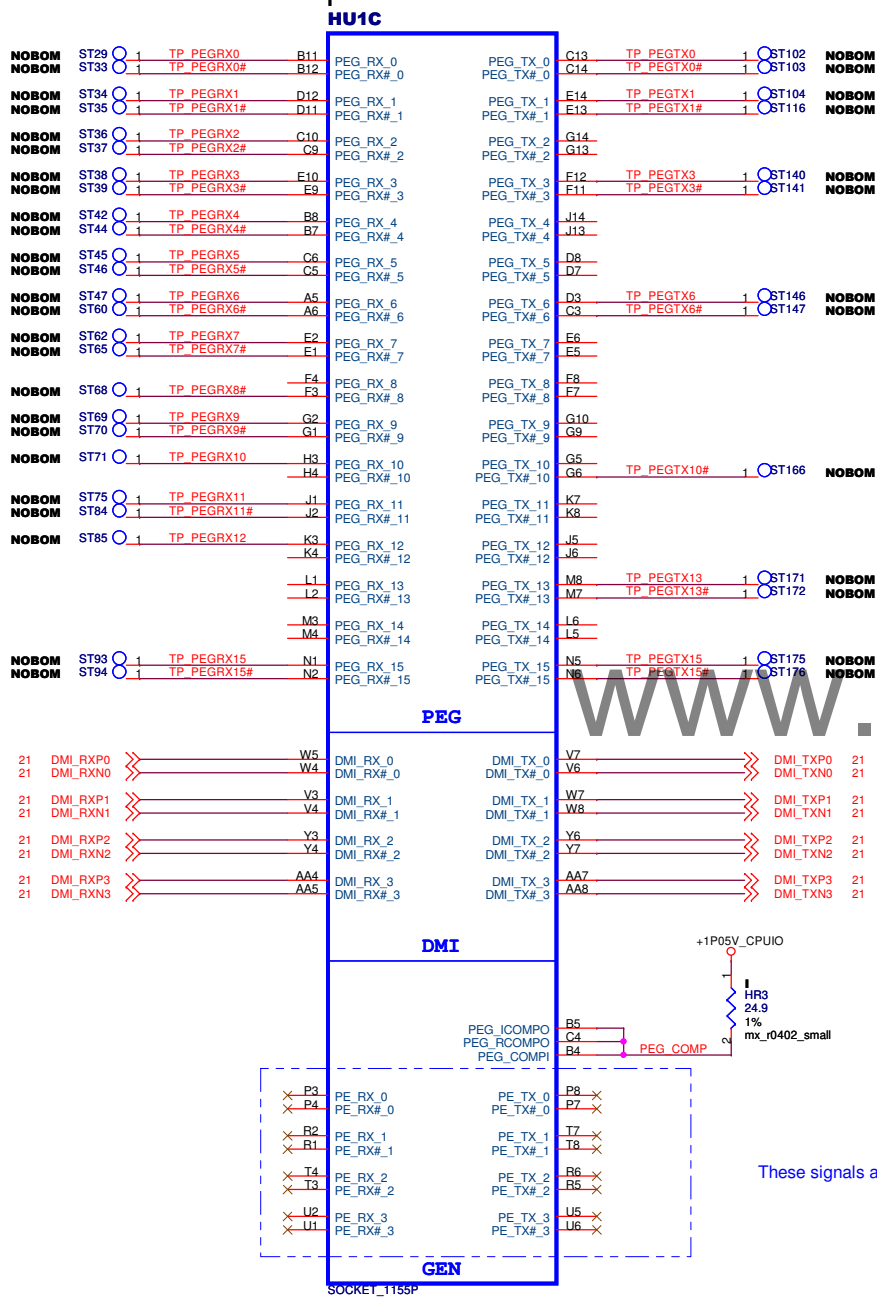
**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : **DDR3\_B 2-6**

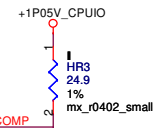
Pegatron Corp. **Engineer:** *KJ Chang*

Size	Project Name	Rev
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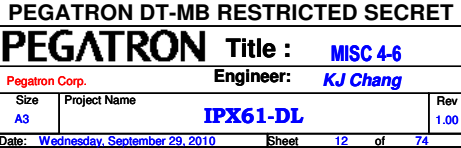
<b>A3</b>	<b>IPX61-DL</b>	<b>1.00</b>
Date: Wednesday, September 20, 2010 Sheet 10 of 34		



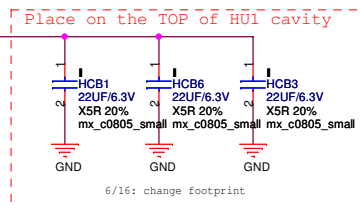
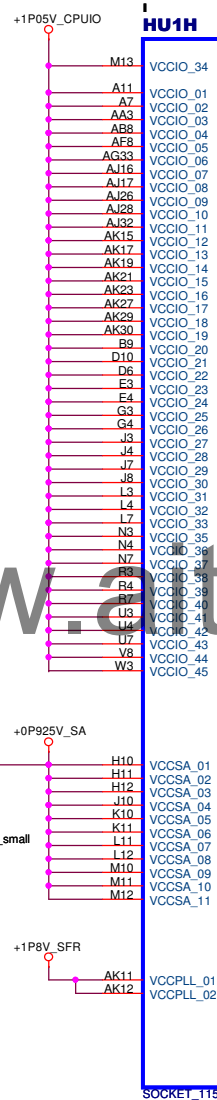
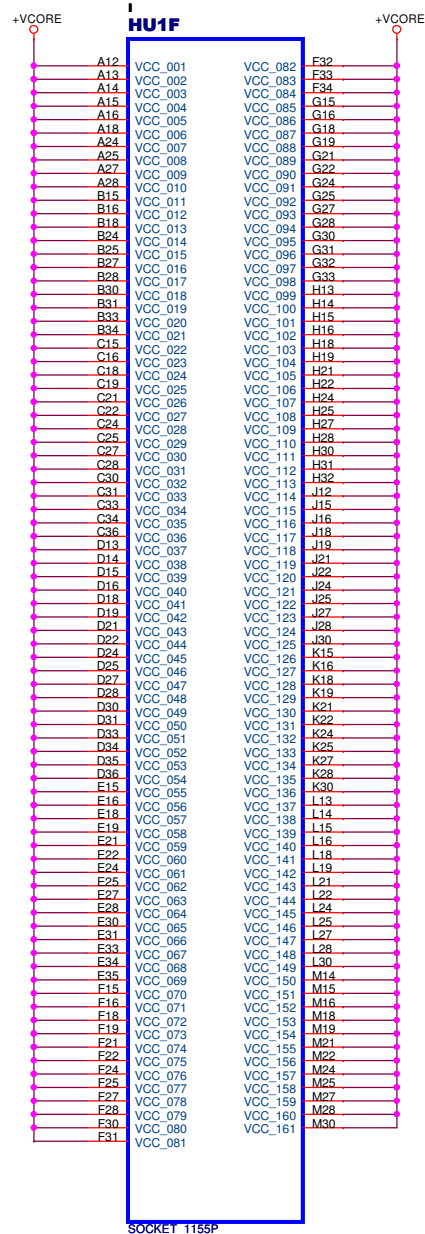
www.aitech1.ru



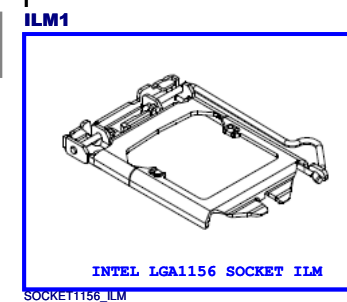
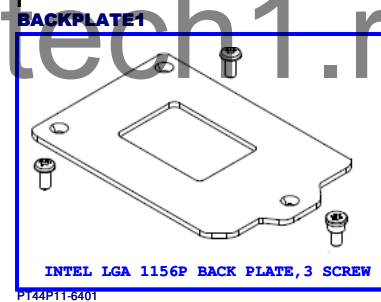
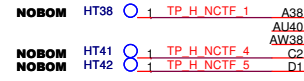
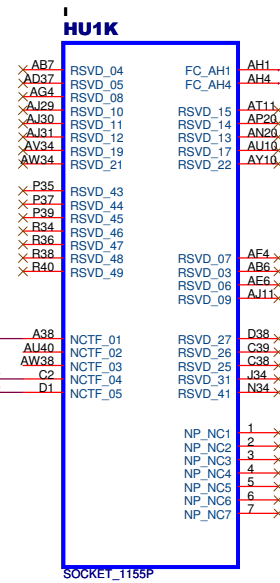
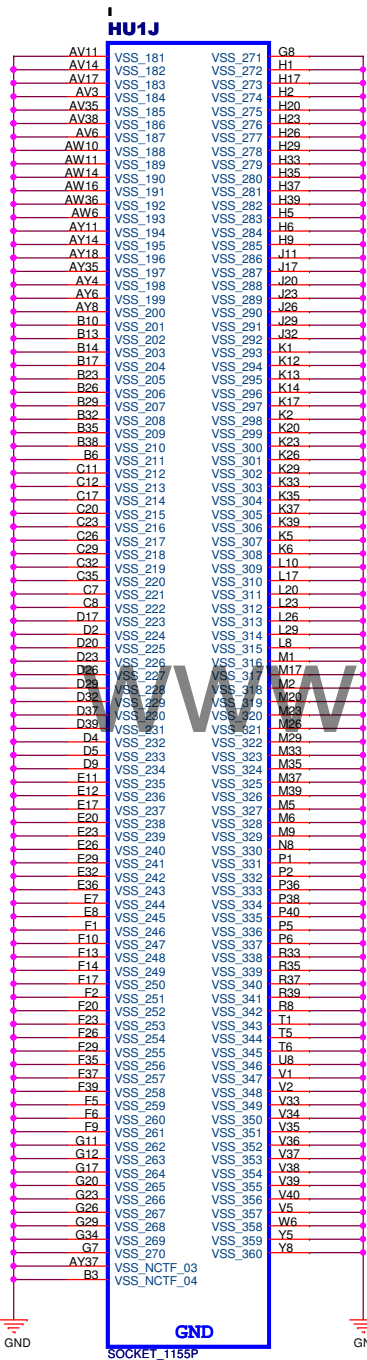
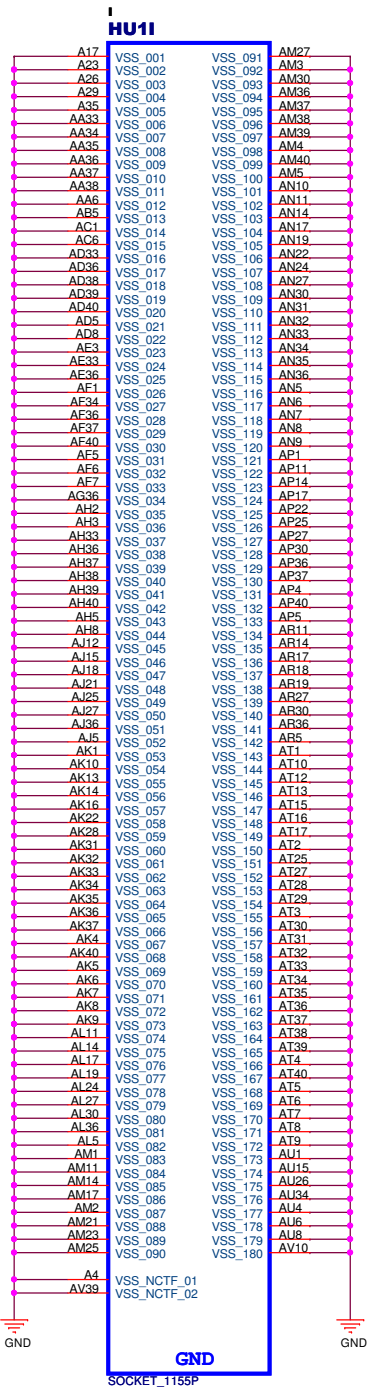
These signals are available for Workstation only.







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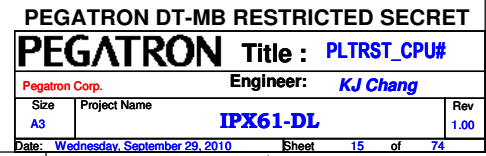
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : VSS 6 - 6

Pegatron Corp. Engineer: KJ Chang

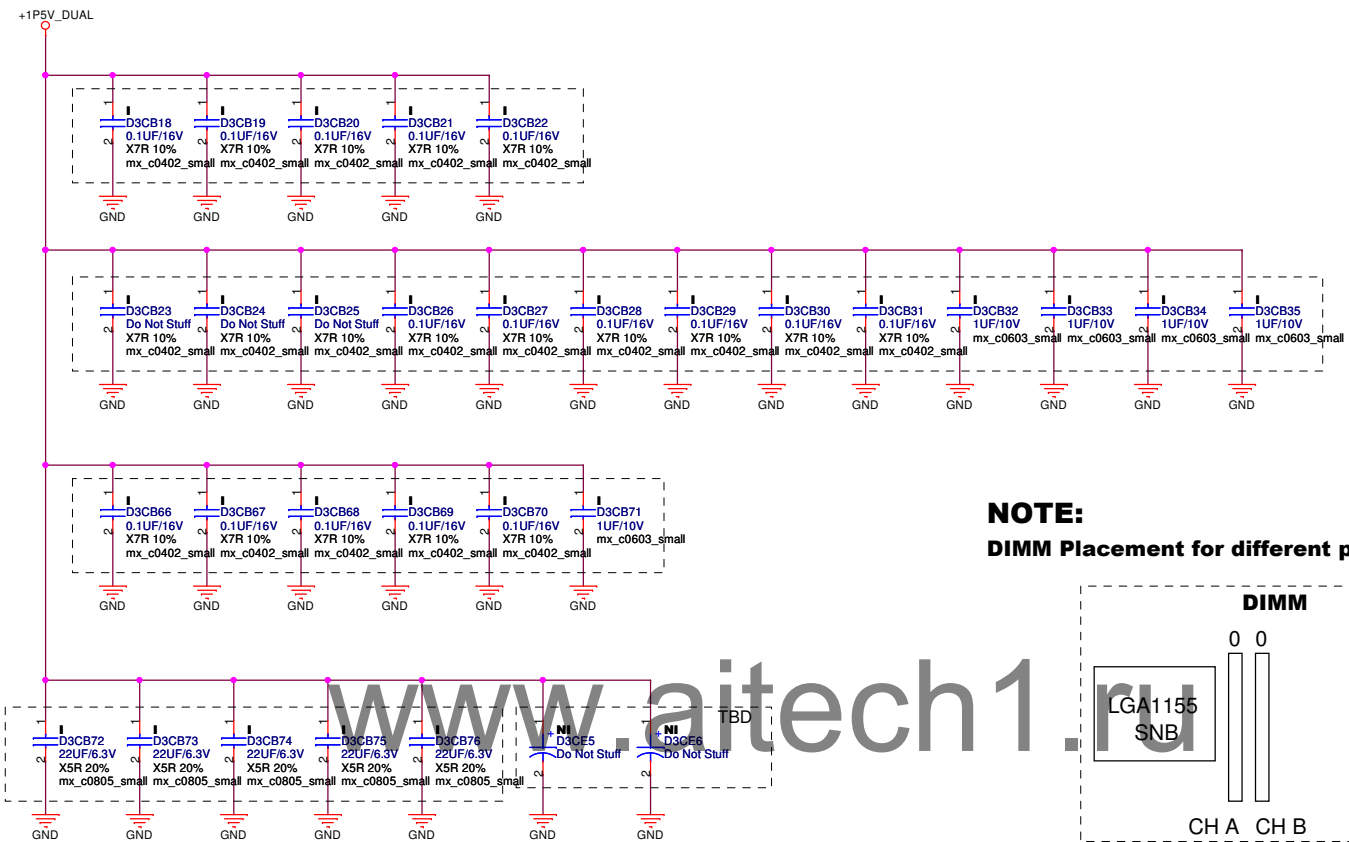
Size A3 Project Name IPX61-DL Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 14 of 74

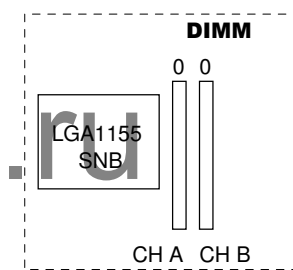


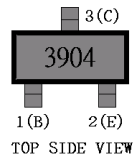






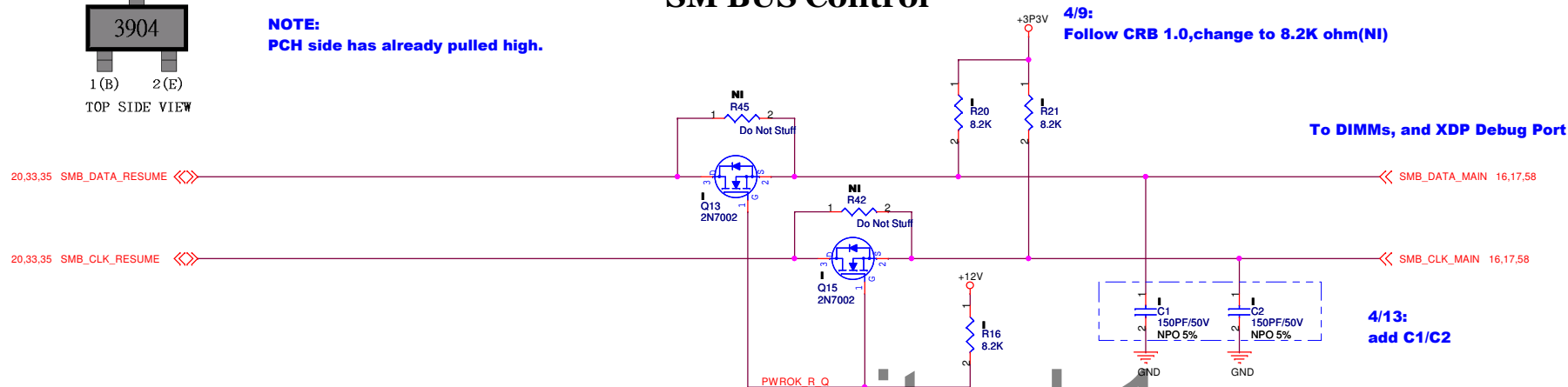
**NOTE:**  
**DIMM Placement for different platform**





**NOTE:**  
PCH side has already pulled high.

## SM BUS Control



**4/9:**  
Follow CRB 1.0, change to 8.2K ohm(NI)

**4/13:**  
add C1/C2

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PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : DDR3 VREF CIRCUIT

Pegatron Corp. Engineer: KJ Chang

Size A3	Project Name IPX61-DL	Rev 1.00
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Date: Wednesday, September 29, 2010 Sheet 19 of 74



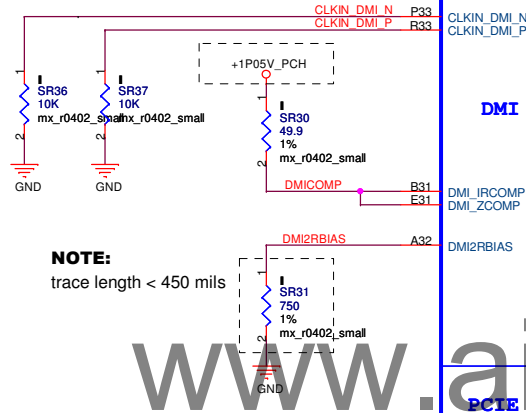
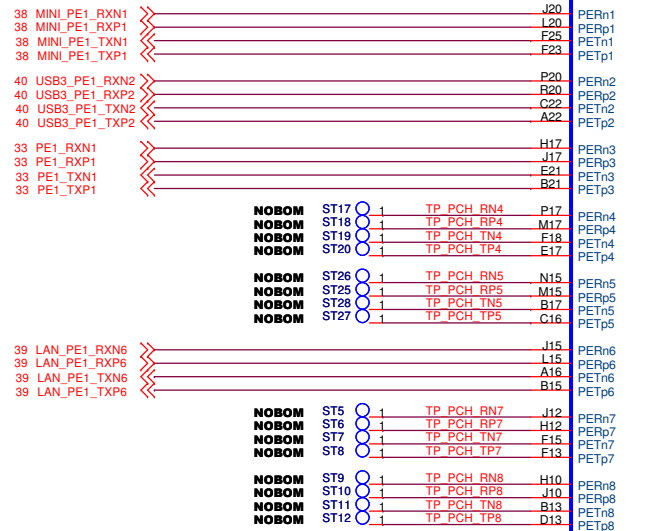
GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

Size A3	Project Name <b>IPX61-DL</b>	Rev 1.00
Date: <b>Wednesday, September 29, 2010</b>		Sheet <b>20</b> of <b>74</b>

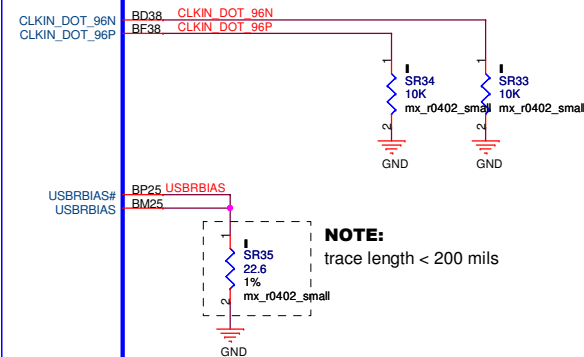


**NOTE:**

Used for DMI, PCIe(Pcie 2.0 jitter spec compliant).

**MINI PCIE SLOT****USB 3.0****X1 SLOT****LAN****SU1B****DMI****USB****PCIE****COUGARPOINT****MINI PCIe Card****MINI PCIe Card****Front USB Dual Header 2****Front USB Dual Header 2****Front USB Dual Header 3****Front USB Dual Header 3****P/S2+USB connector****P/S2+USB connector****Front USB Dual Header 1****Front USB Dual Header 1****NOTE:**

Used for integrated graphics, generate USB backbone, 24MHz HDA bit, and 48MHz clock.



2 PEGATRON DT-MB RESTRICTED SECRET

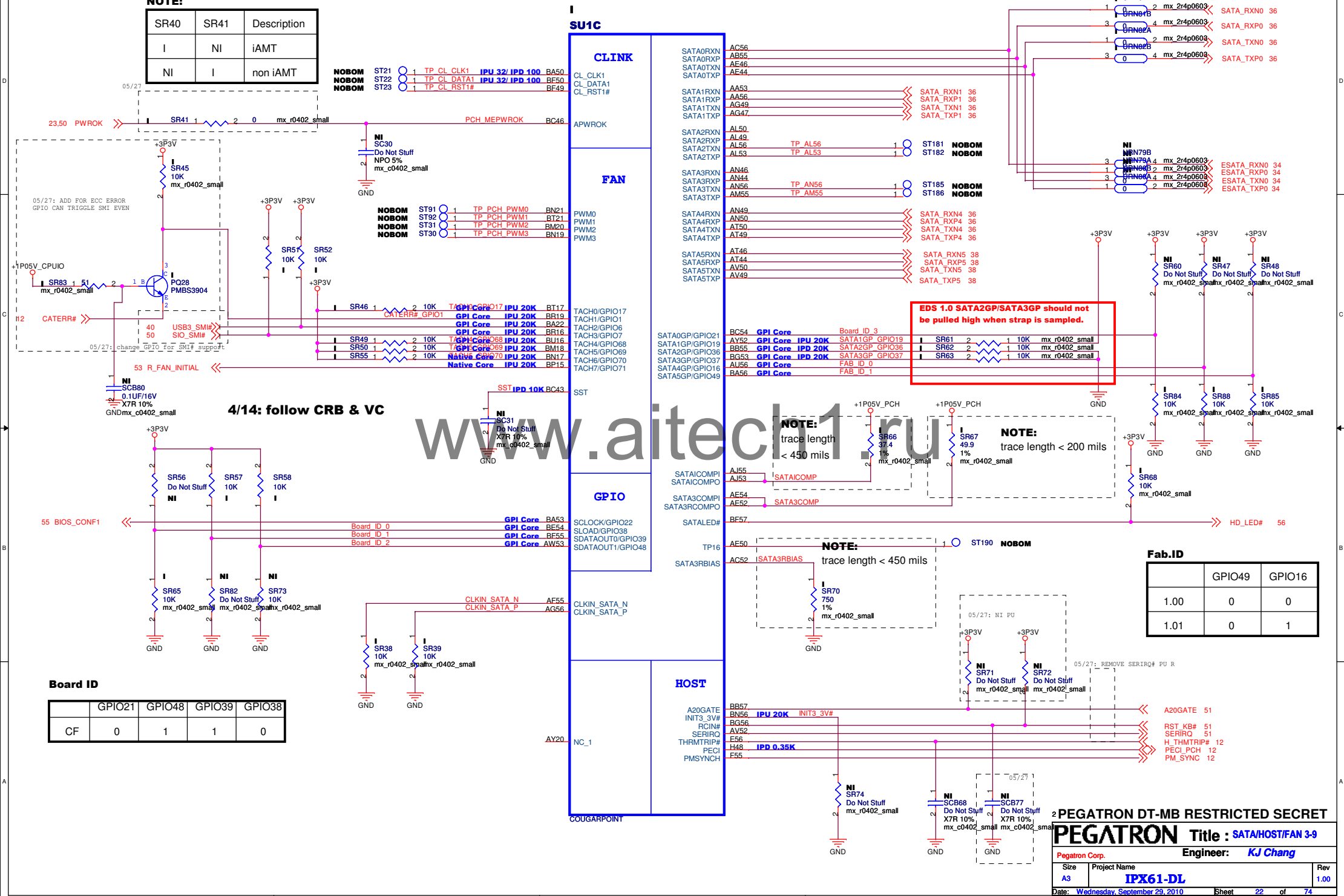
**PEGATRON** Title : PCIE/USB/DMI 2-9

Pegatron Corp. Engineer: KJ Chang

Size A3 Project Name IPX61-DL Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 21 of 74

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT



**NOTE:** HDA\_SYNC  
On-die PLL VR voltage selector.  
Hi: supplied by 1.5V.  
Low: supplied by 1.8V.

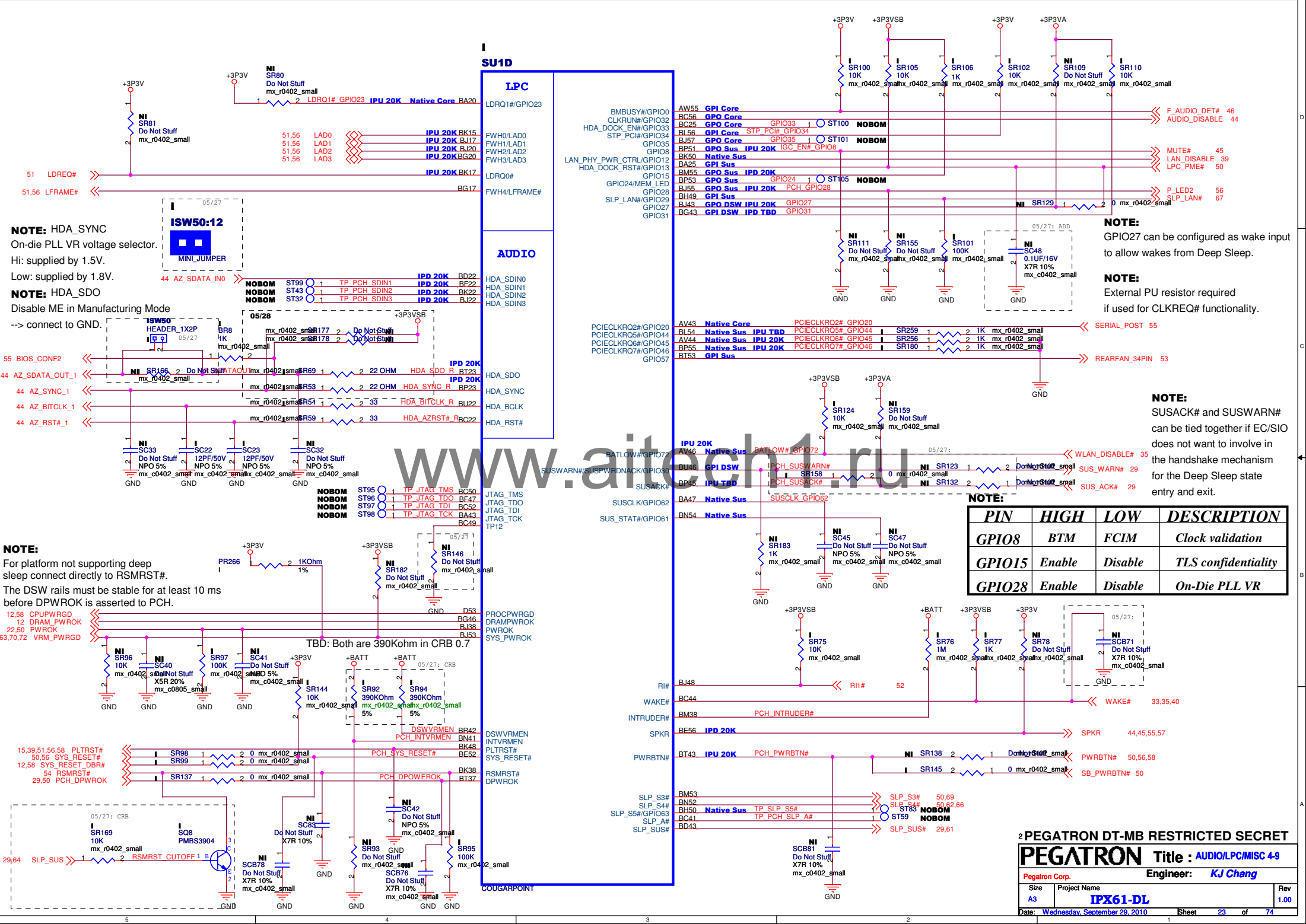
**NOTE:** HDA\_SDO  
Disable ME in Manufacturing Mode  
--> connect to GND.

**NOTE:**  
For platform not supporting deep sleep connect directly to RSMRST#.  
The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.

12,58 CPUWROK  
12 DRAM\_PWROK  
22,50 PWROK  
5,63,70,72 VRM\_PWROK

15,39,51,56,58 PLTRST#  
50,56 SYS\_RESET#  
12,58 SYS\_RESET\_DBR#  
54 RSMRST#  
29,50 PCH\_DPWROK

29,64 SLP\_SUS#



PIN	HIGH	LOW	DESCRIPTION
GPIO8	BTM	FCIM	Clock validation
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR

# SU1E

Y18  
Y17  
AB18  
AB17

TP6  
TP7  
TP8  
TP9

30 VGA\_DDCA\_CLK  
30 VGA\_DDCA\_DATA

AW3  
AW1

CRT\_DDC\_CLK  
CRT\_DDC\_DATA

CRT\_HSYNC  
CRT\_VSYNC

AR4  
AR2

VGA\_HSYNC\_3P3V  
VGA\_VSYNC\_3P3V

SR245  
SR246

2 33 mx\_r0402\_small  
2 33 mx\_r0402\_small

JP20  
JP21  
JP22

2 SHORT\_PIN  
2 NOBOM Do Not Stuff  
2 NOBOM SHORT\_PIN  
2 NOBOM

VGA\_RED\_30  
VGA\_GREEN\_30  
VGA\_BLUE\_30

CRT\_RED  
CRT\_GREEN  
CRT\_BLUE

AN6  
AN2  
AM1

VGA\_RED\_S  
VGA\_GREEN\_S  
VGA\_BLUE\_S

SR247  
SR248  
SR249

150 1%  
150 1%  
150 1%

mx\_r0402\_small  
mx\_r0402\_small  
mx\_r0402\_small

GND  
GND  
GND

DAC\_IREF  
CRT\_IRTN

AT3  
AM6

DACREFSET

GND

SR131  
1K 1%  
mx\_r0402\_small

GND

NOTE:  
Place RGB resistors close to PCH within 250mils  
Replace DACREFSET resistor  
close to PCH within 500mils

DDPB\_OP  
DDPB\_ON  
DDPB\_1P  
DDPB\_1N  
DDPB\_2P  
DDPB\_2N  
DDPB\_3P  
DDPB\_3N

R14  
R12  
M11  
M12  
H8  
K8  
L5  
M3

DVI\_TMDSB\_DATA2\_32  
DVI\_TMDSB\_DATA2#\_32  
DVI\_TMDSB\_DATA1\_32  
DVI\_TMDSB\_DATA1#\_32  
DVI\_TMDSB\_DATA0\_32  
DVI\_TMDSB\_DATA0#\_32  
DVI\_TMDSB\_CLK\_32  
DVI\_TMDSB\_CLK#\_32

SDVO\_INTN  
SDVO\_INTN

U2  
T3

IPD 50  
IPD 50

TP SDVO INTN  
TP SDVO INTN

ST78  
ST79

NOBOM  
NOBOM

SDVO\_STALLP  
SDVO\_STALLN

W3  
U5

IPD 50  
IPD 50

TP SDVO STALLP  
TP SDVO STALLN

ST110  
ST111

NOBOM  
NOBOM

SDVO\_TVCLKINP  
SDVO\_TVCLKINN

U8  
U9

IPD 50  
IPD 50

TP SDVO STALLP  
TP SDVO STALLN

ST112  
ST113

NOBOM  
NOBOM

DDPC\_OP  
DDPC\_ON  
DDPC\_1P  
DDPC\_1N  
DDPC\_2P  
DDPC\_2N  
DDPC\_3P  
DDPC\_3N

L2  
J3  
G2  
G4  
E3  
E5  
E4  
E2

TP DDPC OP  
TP DDPC ON  
TP DDPC 1P  
TP DDPC 1N  
TP DDPC 2P  
TP DDPC 2N  
TP DDPC 3P  
TP DDPC 3N

ST114  
ST115  
ST117  
ST118  
ST119  
ST120  
ST151  
ST187

NOBOM  
NOBOM  
NOBOM  
NOBOM  
NOBOM  
NOBOM  
NOBOM  
NOBOM

DDPD\_OP  
DDPD\_ON  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

D5  
B5  
C6  
D7  
B7  
C9  
E11  
B11

HDMI\_TMDSB\_DATA2\_34  
HDMI\_TMDSB\_DATA2#\_34  
HDMI\_TMDSB\_DATA1\_34  
HDMI\_TMDSB\_DATA1#\_34  
HDMI\_TMDSB\_DATA0\_34  
HDMI\_TMDSB\_DATA0#\_34  
HDMI\_TMDSB\_CLK\_34  
HDMI\_TMDSB\_CLK#\_34

DVI-D

HDMI

2 PEGATRON DT-MB RESTRICTED SECRET

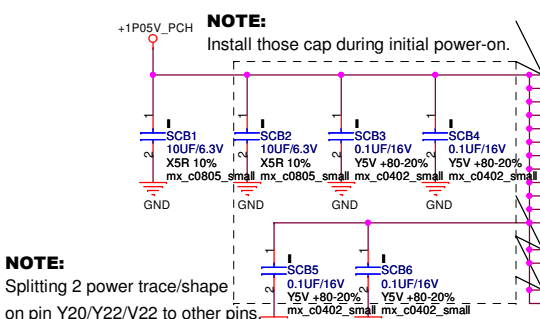
PEGATRON Title : VGA/DP/HDMI 5-9

Pegatron Corp. Engineer: KJ Chang

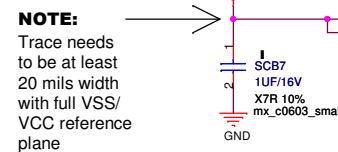
Size A3 Project Name IPX61-DL Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 24 of 74

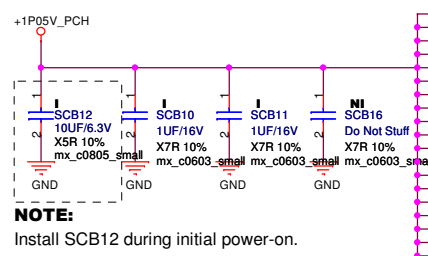
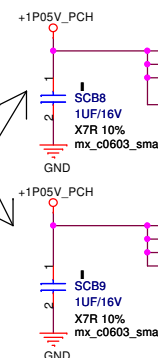




**NOTE:**  
Splitting 2 power trace/shape on pin Y20/Y22/V22 to other pins.



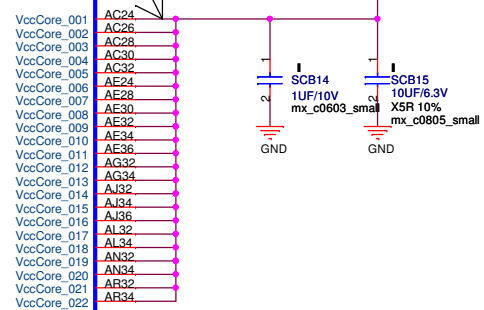
**NOTE:**  
Splitting 2 power trace/shape



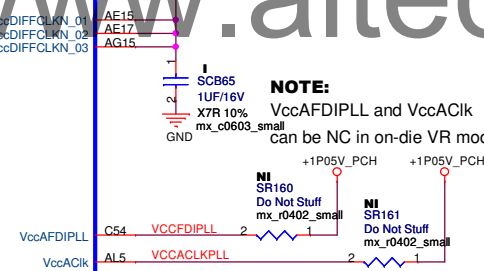
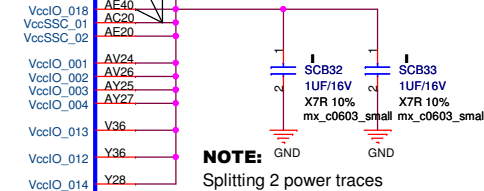
**SU1G**

VccIO\_024  
VccIO\_025  
VccIO\_026  
VccIO\_027  
VccIO\_028  
VccIO\_029  
VccIO\_030  
VccIO\_031  
VccIO\_032  
VccIO\_033  
VccIO\_034  
VccIO\_035  
VccIO\_036  
VccIO\_037  
VccIO\_022  
VccIO\_023  
VccIO\_036  
VccIO\_037  
VccIO\_008  
VccIO\_009  
VccIO\_010  
VccIO\_019  
VccIO\_020  
VccIO\_021  
VccIO\_007  
VccIO\_011  
VccASW\_004  
VccASW\_005  
VccASW\_006  
VccASW\_007  
VccASW\_008  
VccASW\_009  
VccASW\_010  
VccASW\_011  
VccASW\_012  
VccASW\_013  
VccASW\_014  
VccASW\_015  
VccASW\_016  
VccASW\_017  
VccASW\_018  
VccASW\_019  
VccASW\_020  
VccASW\_021  
VccASW\_022  
VccASW\_023  
VccASW\_003  
VccASW\_002  
VccASW\_001

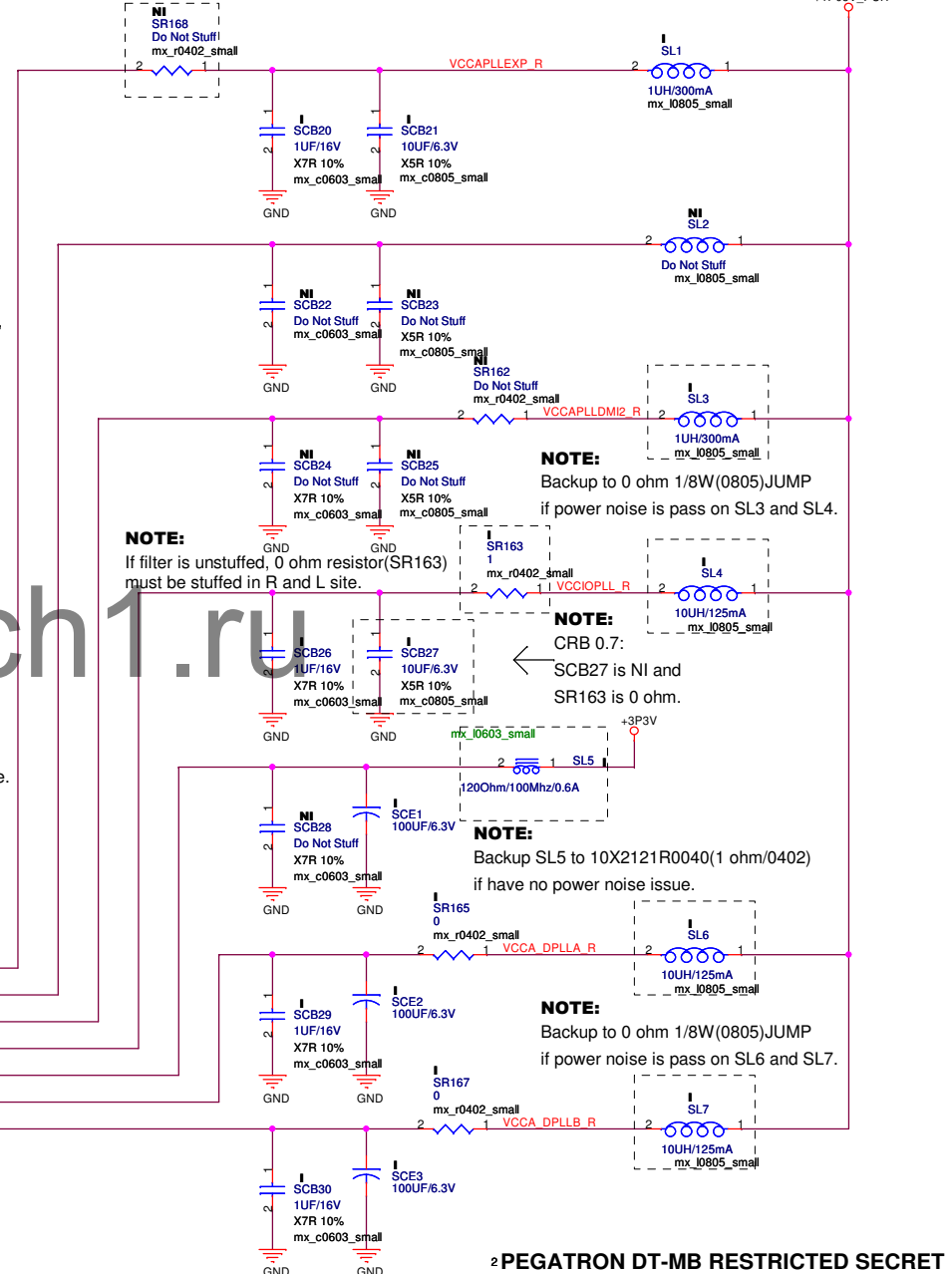
**COUGARPOINT**



**NOTE:**  
Splitting 2 power trace/shape on pins AV24/AV26 to AY25/AY27, and AE40 to AG38/AG40.



**NOTE:**  
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC in On-Die VR mode.





**NOTE:**

Place SCB59 and SCB66 near pin AU20,  
SCB60 near pin AL38,  
SCB61 and SCB67 near BC17.

**NOTE:**

Splitting 2 power trace/shape on  
pin AV20/AU20 and AU22.

**NOTE:**

Install SCB58 during initial power-on.

**NOTE:**

Install SCB31 during initial power-on.

**NOTE:**

Splitting 2 power trace/shape on  
pin AV28, AY31/AY33, and AV30/AV32.

**NOTE:**

Place SCB53 near pin BT35, SCB54 near pin U31,  
and SCB69 near pin AV30/AT40.

**NOTE:**

Place SCB56 near PCH within 40mils.

**NOTE:**

Just for measurement.

CRB 0.7 is 1uF

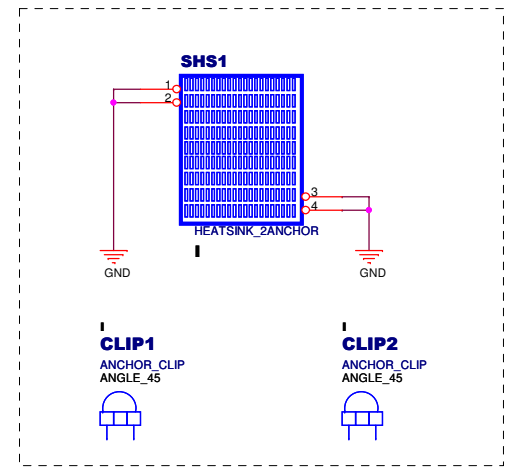
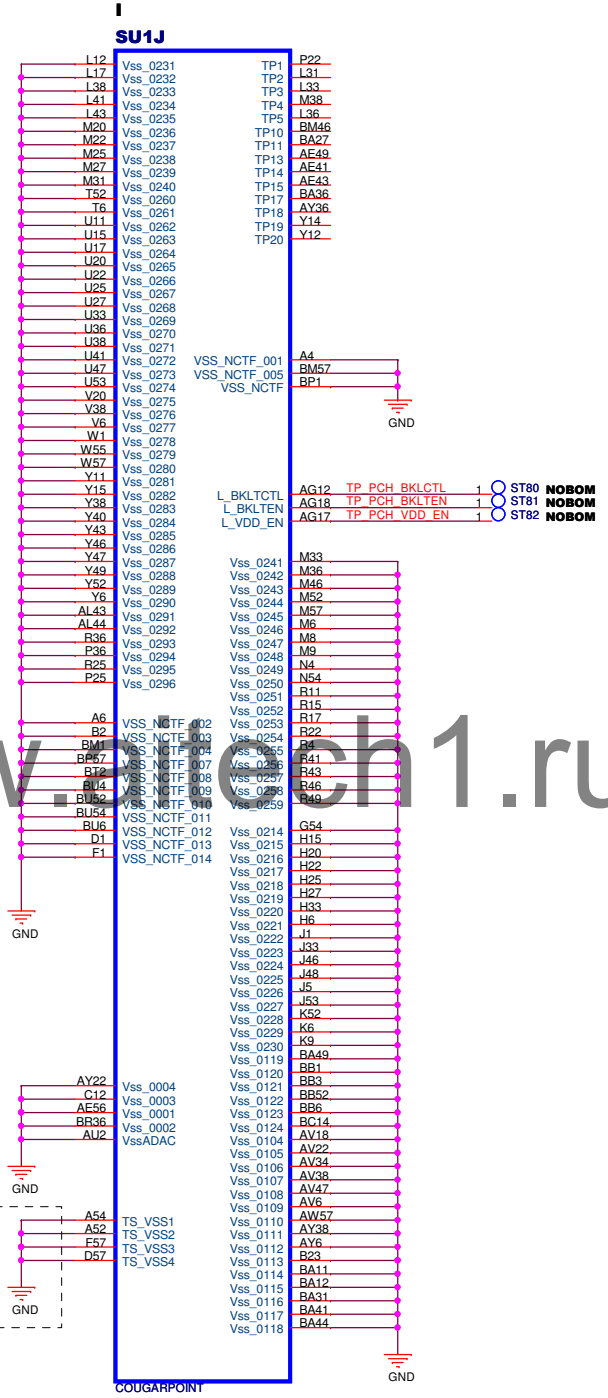
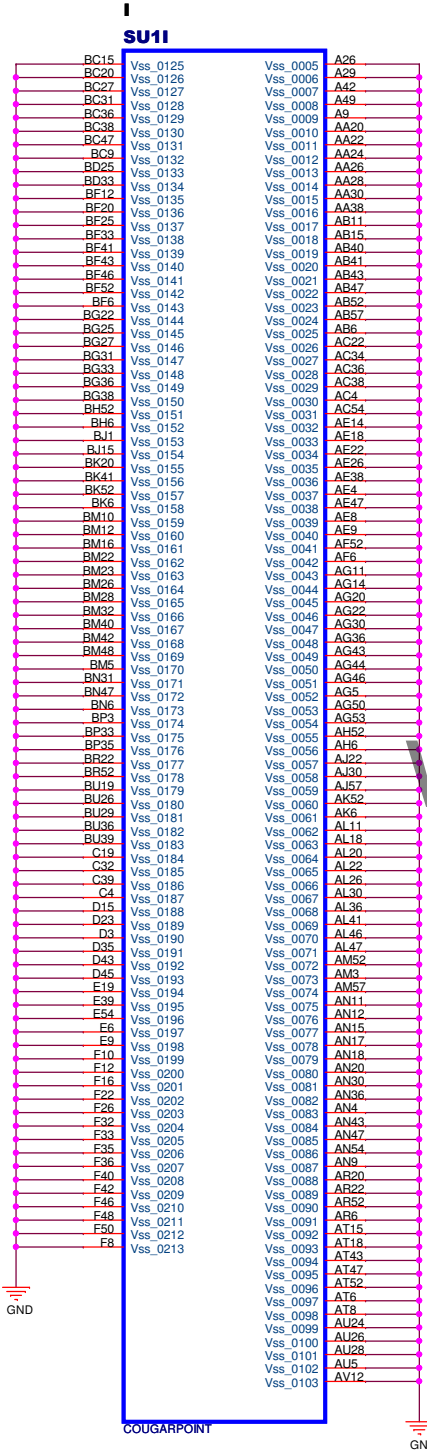
2 PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : VCCSUS 8-9

Pegatron Corp. Engineer: KJ Chang

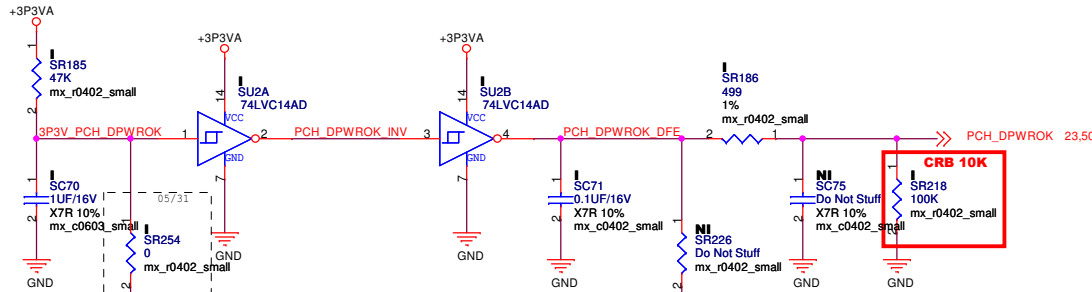
Size A3 Project Name IPX61-DL Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 27 of 74



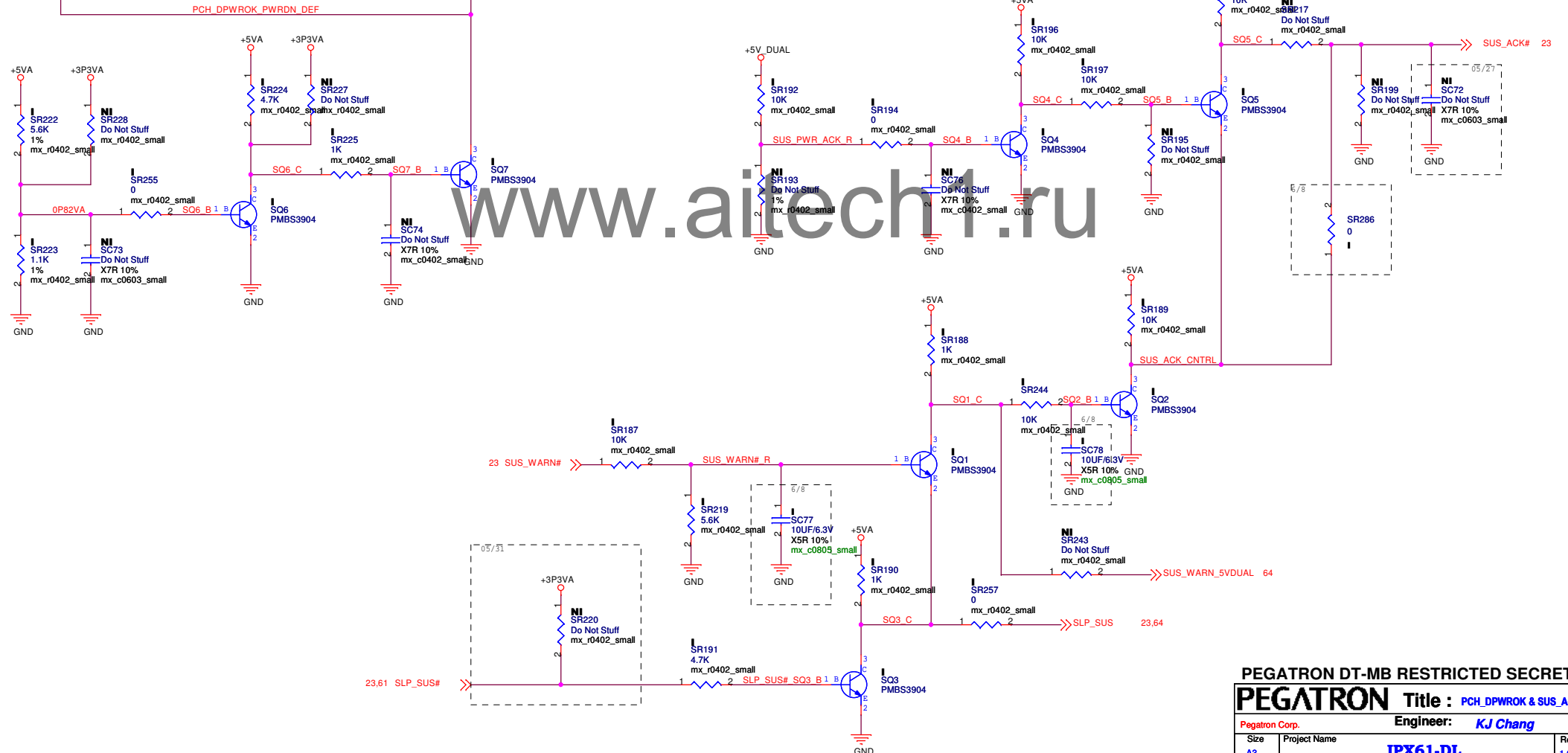


**PCH\_DPWROK**



**SUS\_ACK#**

**NOTE:**  
Check voltage level of SUS\_ACK# of PCH  
and decide resistor value of SR199.



**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : PCH\_DPWROK & SUS\_ACK#

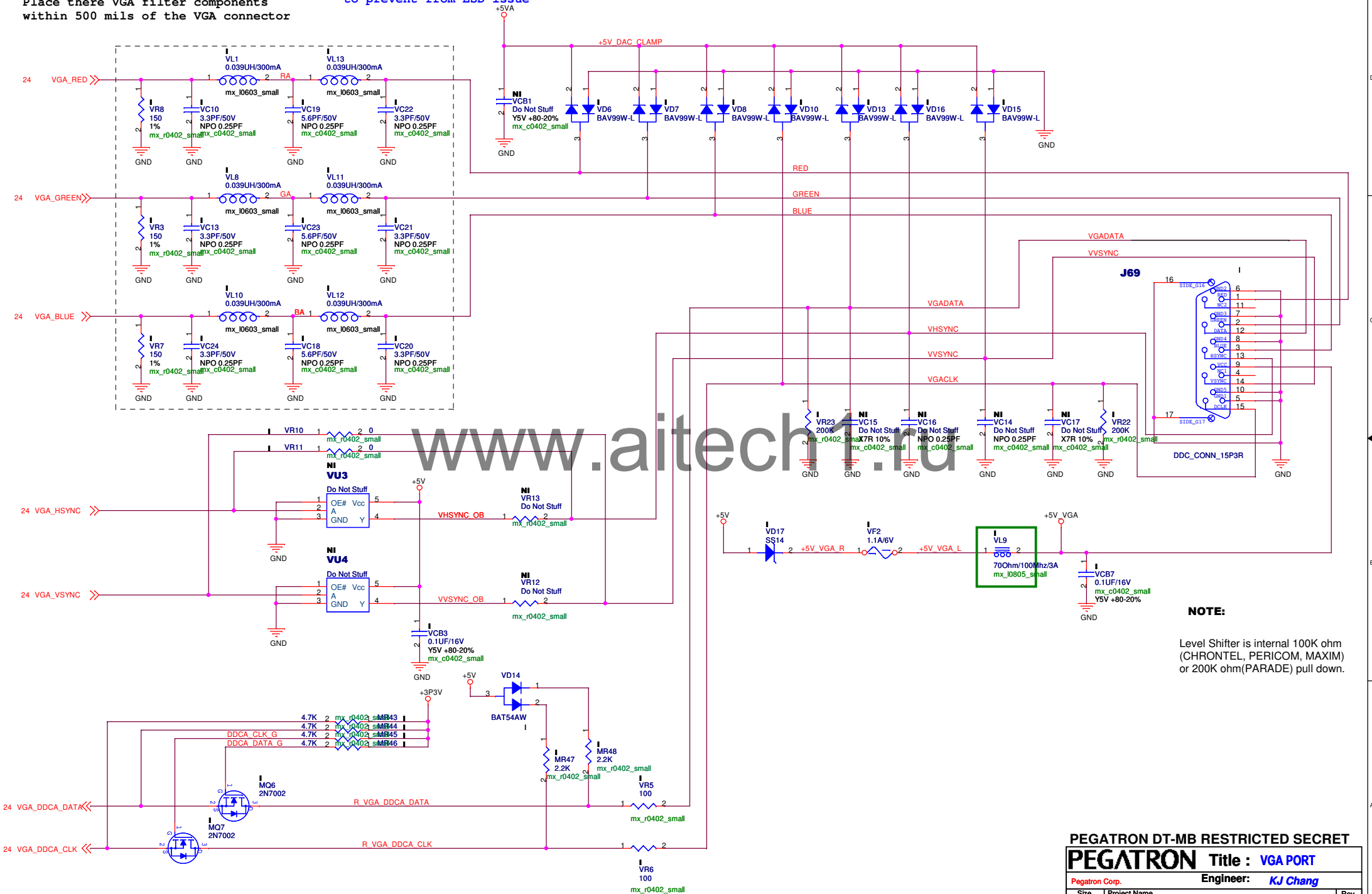
Pegatron Corp.		Engineer: <i>KJ Chang</i>	
Size A3	Project Name <b>IPX61-DL</b>		Rev 1.00
Date: <u>Wednesday, September 29, 2010</u>		Sheet <u>29</u> of <u>74</u>	

**NOTE:**

Place there VGA filter components  
within 500 mils of the VGA connector

**NOTE:**

Install the VD1/VD2/VD3/VD4/VD5 diode  
to prevent from ESD issue



PEGATRON DT-MB RESTRICTED SECRET

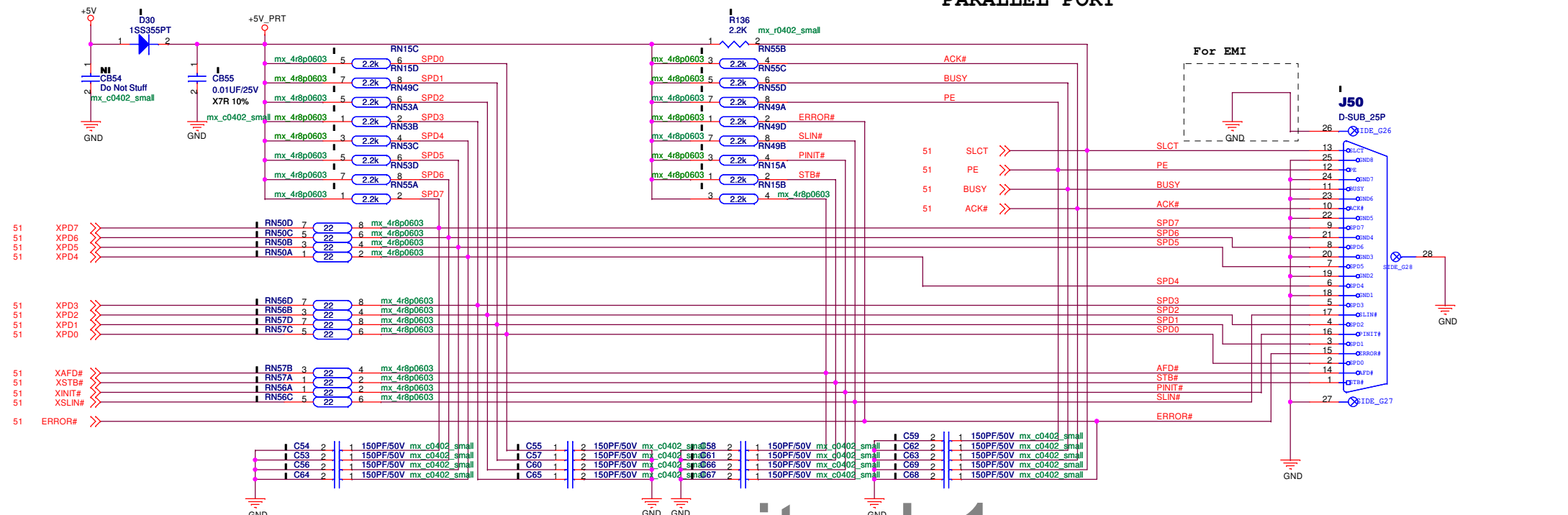
**PEGATRON** Title : **VGA PORT**

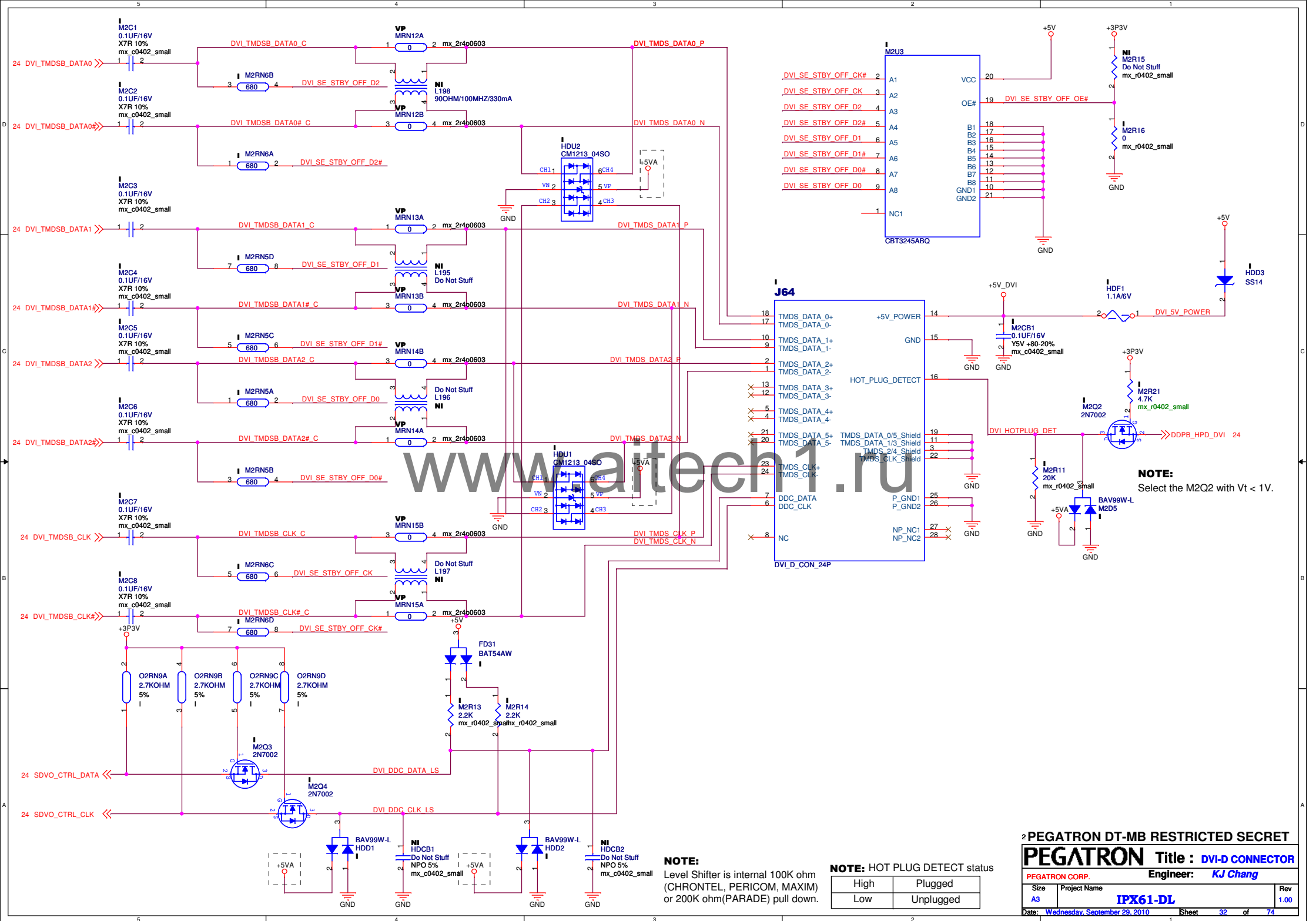
Pegatron Corp. Engineer: **KJ Chang**

Size A3 Project Name **IPX61-DL** Rev 1.00

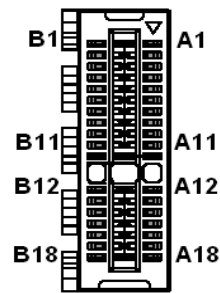
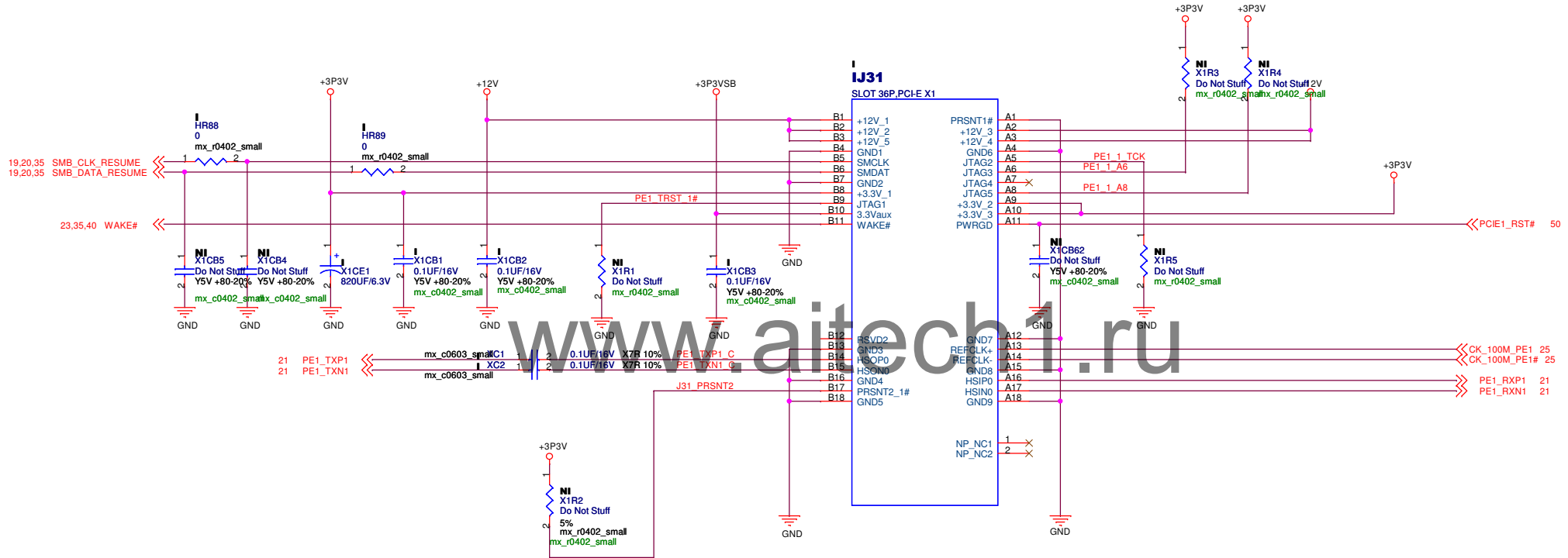
Date: Wednesday, September 29, 2010 Sheet 30 of 74

# PARALLEL PORT

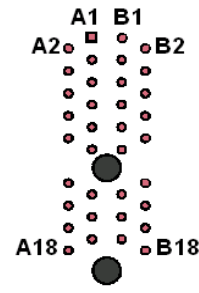




# PCI Express x1 SLOT



TOP SIDE VIEW



BOTTOM SIDE VIEW

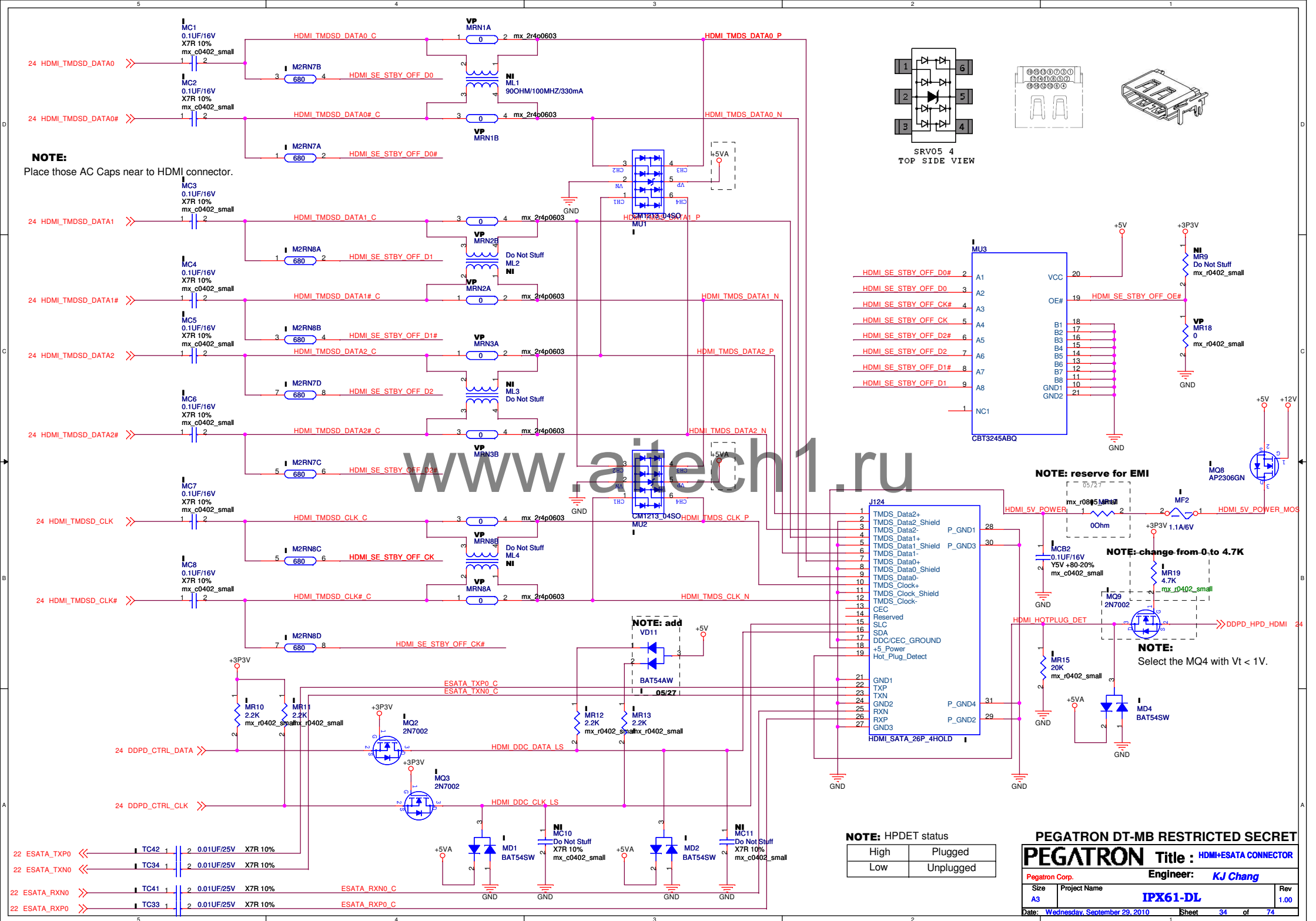
PEGATRON DT-MB RESTRICTED SECRET

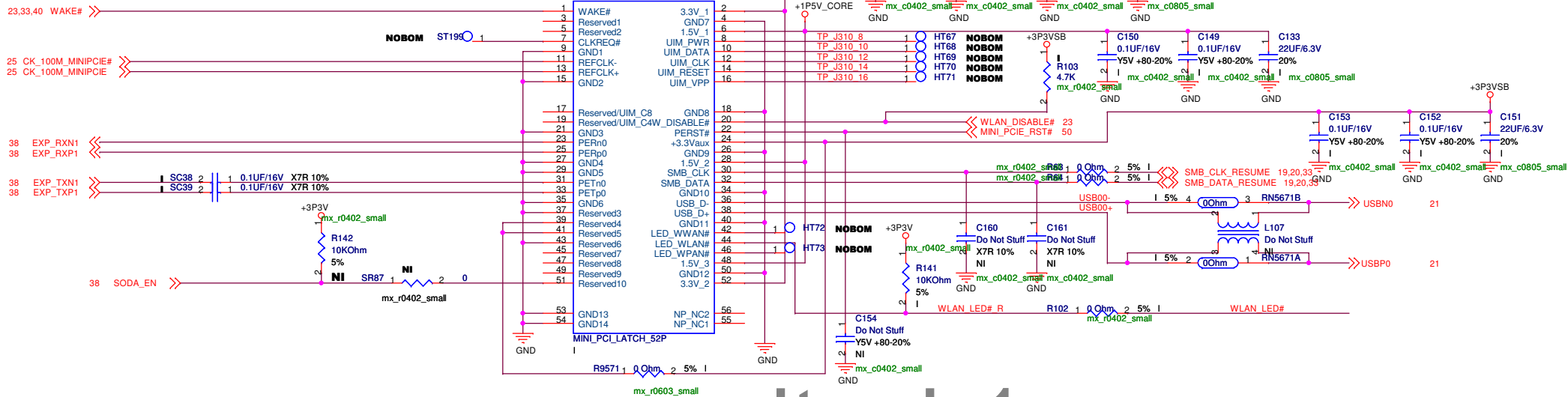
**PEGATRON** Title : **PCI EXPRESS X1**

Pegatron Corp. Engineer: **KJ Chang**

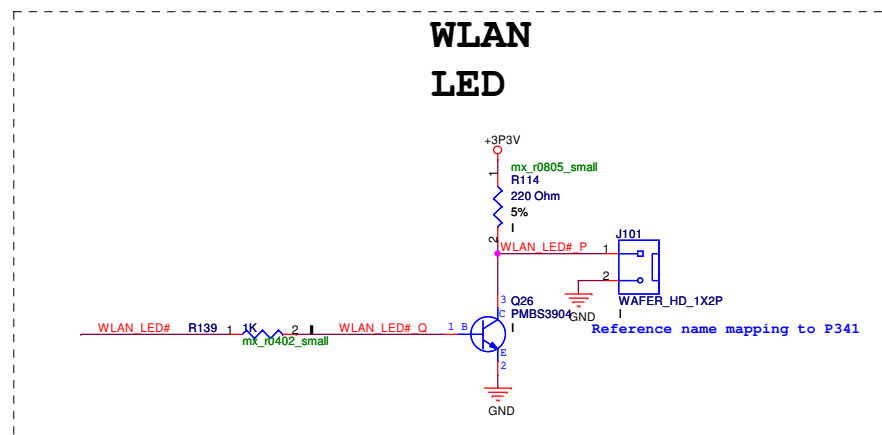
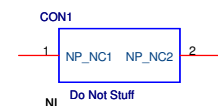
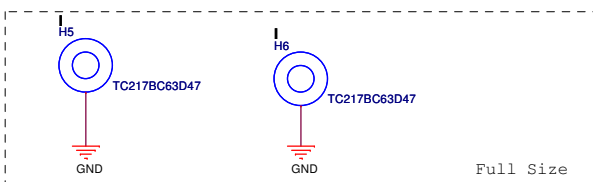
Size A3	Project Name <b>IPX61-DL</b>	Rev 1.00
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Date: Wednesday, September 29, 2010 Sheet 33 of 74



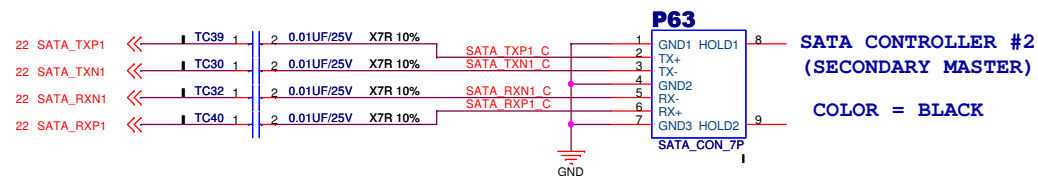
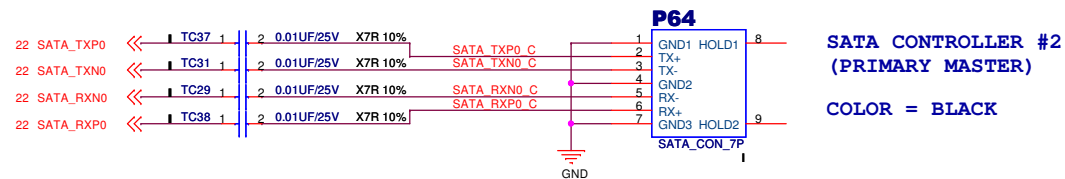


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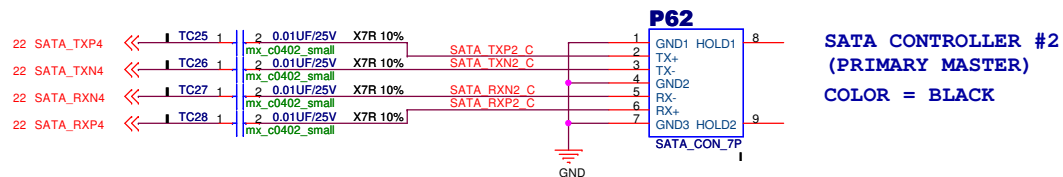


# SATA CONNECTOR

COLOR = Black



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PEGATRON DT-MB RESTRICTED SECRET

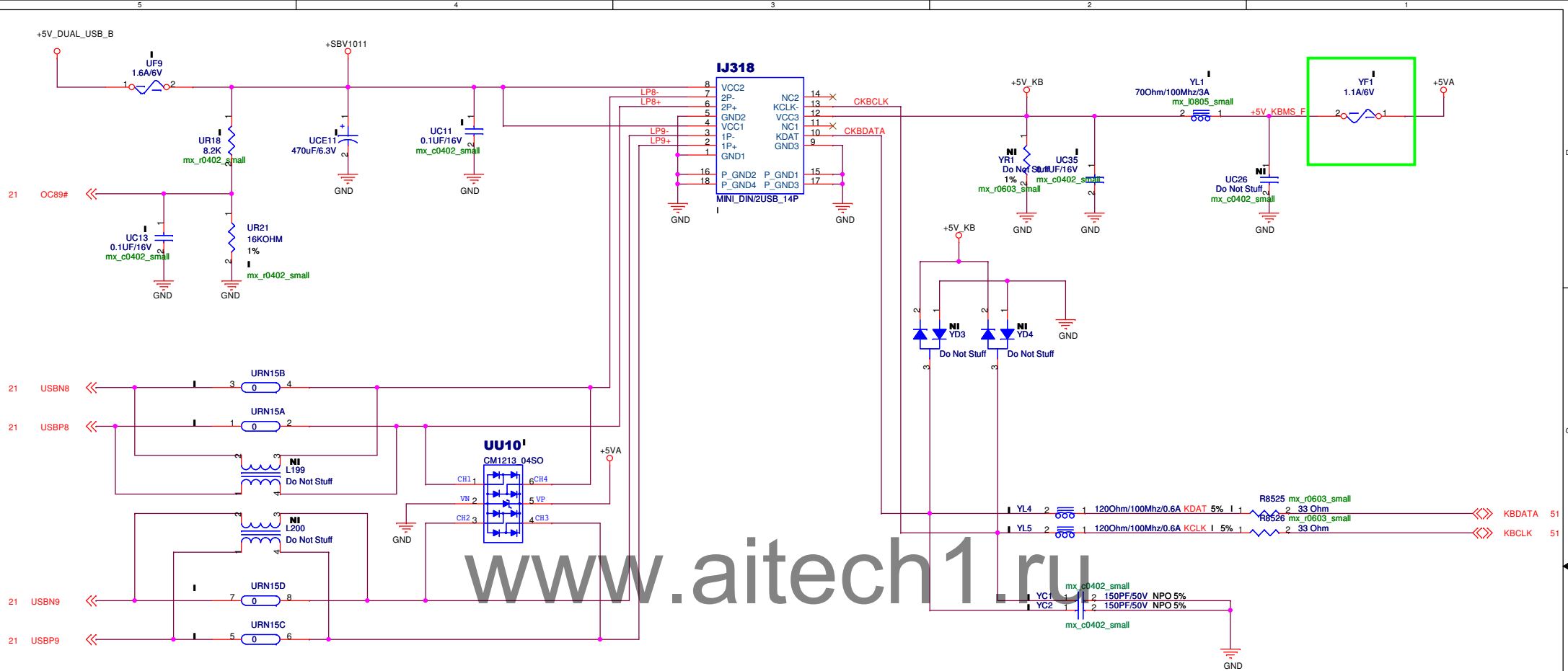
**PEGATRON** Title : **SATA CONNECTOR**

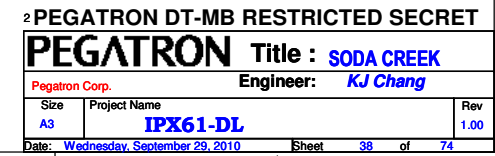
Pegatron Corp. Engineer: **KJ Chang**

Size A3	Project Name <b>IPX61-DL</b>	Rev 1.00
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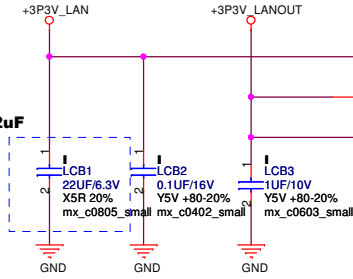
Date: Wednesday, September 29, 2010 Sheet 36 of 74



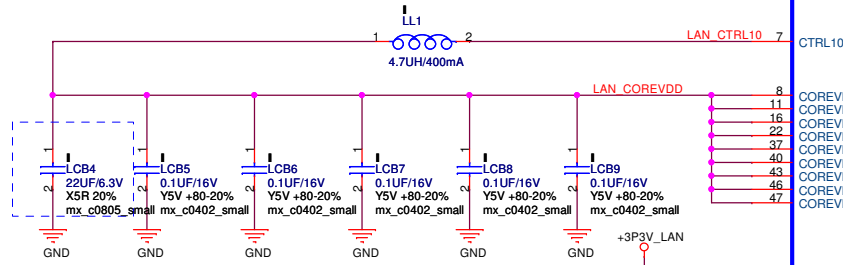




04/14: LCB1 change from 10uF to 22uF



04/26: LCB1 change from 10uF to 22uF

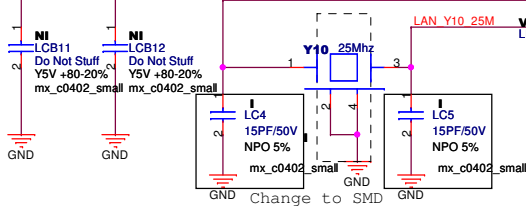


15,23,51,56,58 PLTRST#

25 CK\_100M\_LAN  
25 CK\_100M\_LAN#

21 LAN\_PE1\_RXP6  
21 LAN\_PE1\_RXN6  
21 LAN\_PE1\_TXP6  
21 LAN\_PE1\_TXN6

20 SML0\_LAN\_CLK  
20 SML0\_LAN\_DATA



LU1

MDI\_PLUS[0]  
MDI\_MINUS[0]  
MDI\_PLUS[1]  
MDI\_MINUS[1]  
MDI\_PLUS[2]  
MDI\_MINUS[2]  
MDI\_PLUS[3]  
MDI\_MINUS[3]

LED[2]  
LED[1]  
LED[0]

GPIO[6]  
GPIO[1]

TCK  
TMS  
TDI  
TDO

TEST\_ENABLE  
RBIA5

GND1  
GND2  
GND3  
GND4  
GND5  
GND6  
GND7  
GND8

13  
14  
17  
18  
20  
21  
23  
24

8  
11  
16  
22  
37  
40  
43  
46  
47

35  
33  
32  
34

30  
12

49  
50  
51  
52  
53  
54  
55  
56  
57

LAN\_MDIO\_P  
LAN\_MDIO\_N  
LAN\_MDIO\_P  
LAN\_MDIO\_N  
LAN\_MDIO\_P  
LAN\_MDIO\_N  
LAN\_MDIO\_P  
LAN\_MDIO\_N

LINK\_100#  
LINK\_1000#  
LAN\_ACT#

GLAN\_TCK  
GLAN\_TMS  
GLAN\_TDI  
GLAN\_TDO

LAN\_TEST\_ENABLE  
LAN\_RBIA5

LR19  
LR20

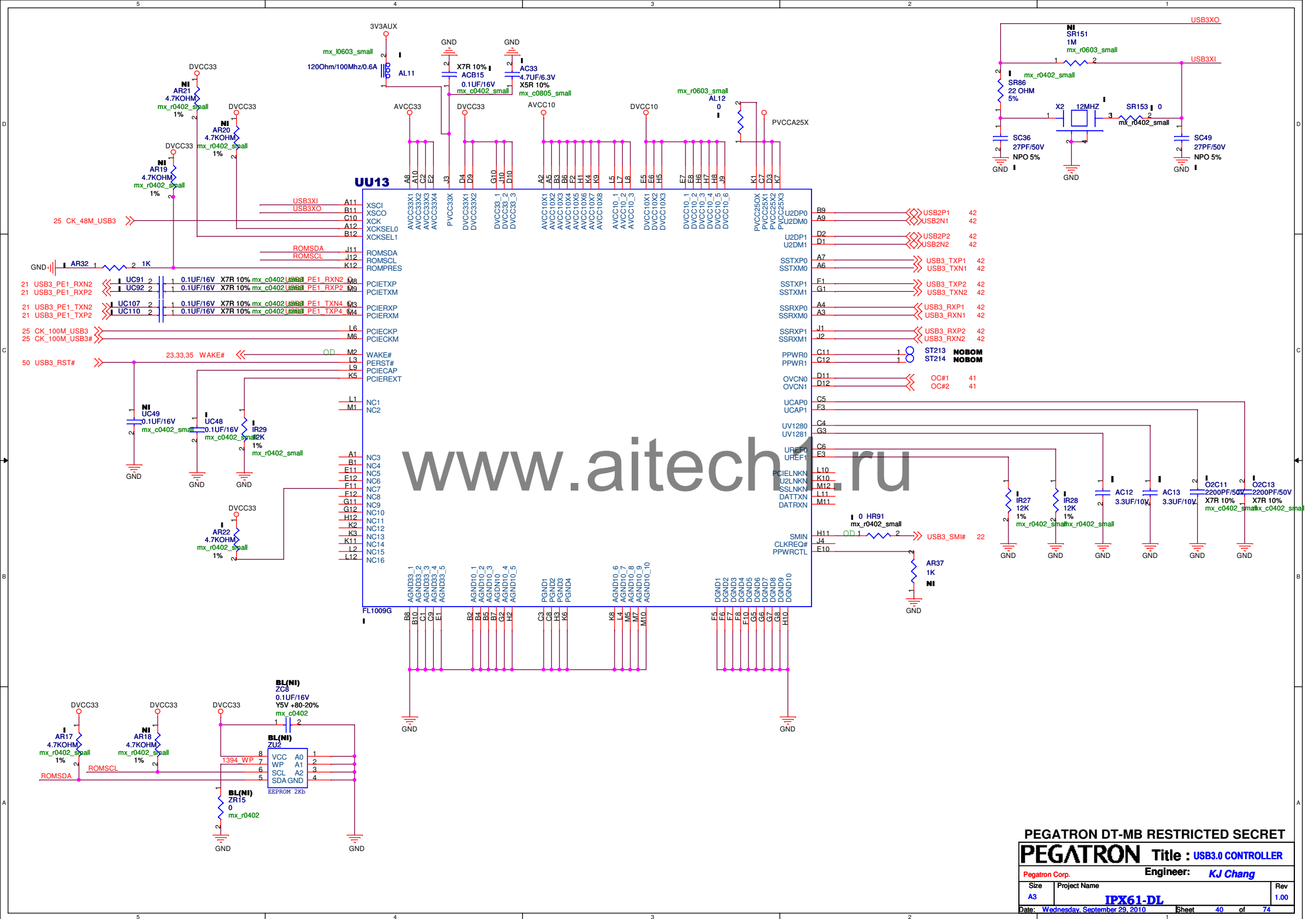
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LEWISVILLE 82579

Pegatron Corp. Engineer: KJ Chang

Size A3 Project Name IPX61-DL Rev 1.00

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PEGATRON DT-MB RESTRICTED SECRET

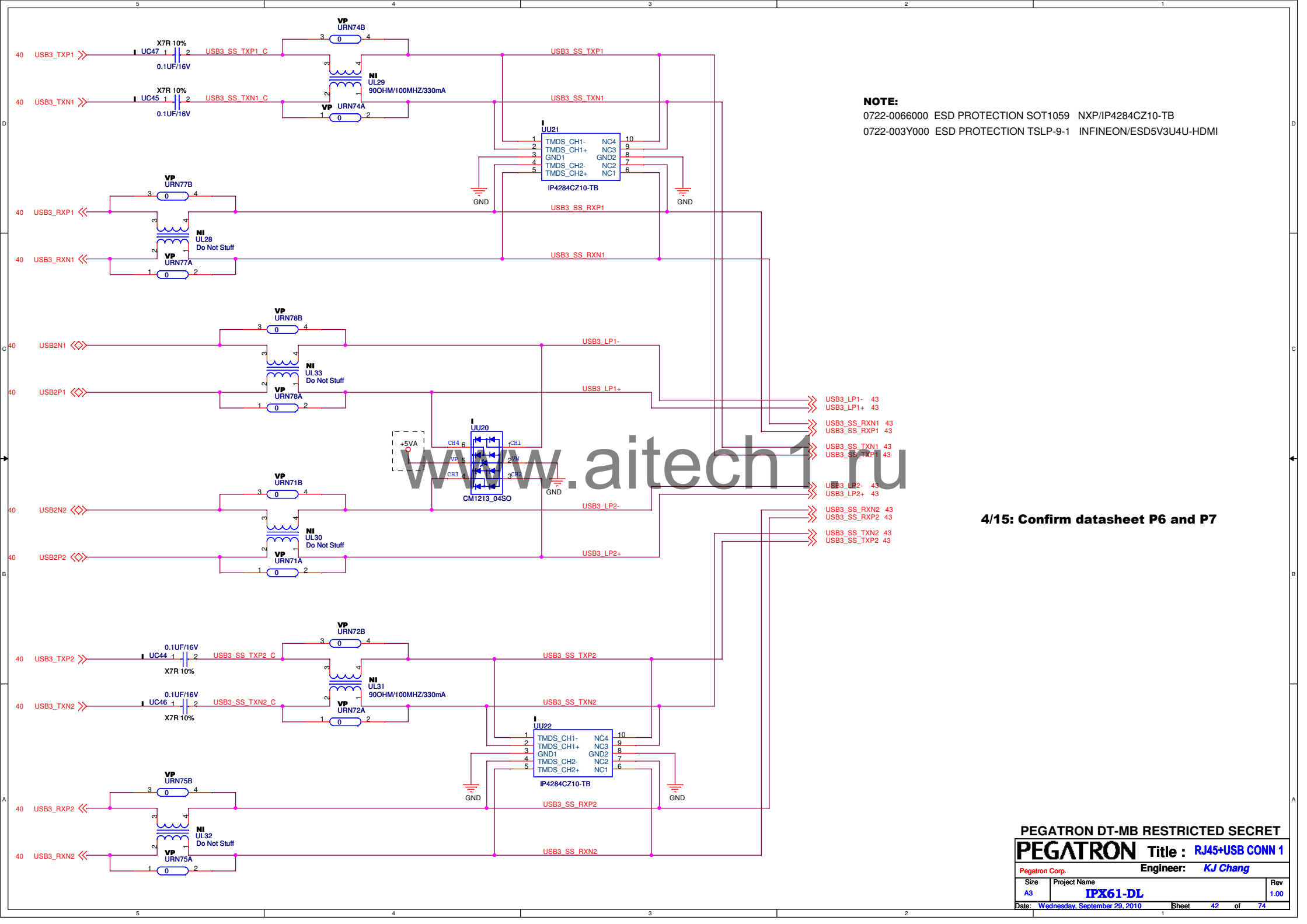
PEGATRON Title : USB3.0 CONTROLLER

Pegatron Corp. Engineer: KJ Chang

Size A3 Project Name IPX61-DL

Date: Wednesday, September 29, 2010 Sheet 40 of 74





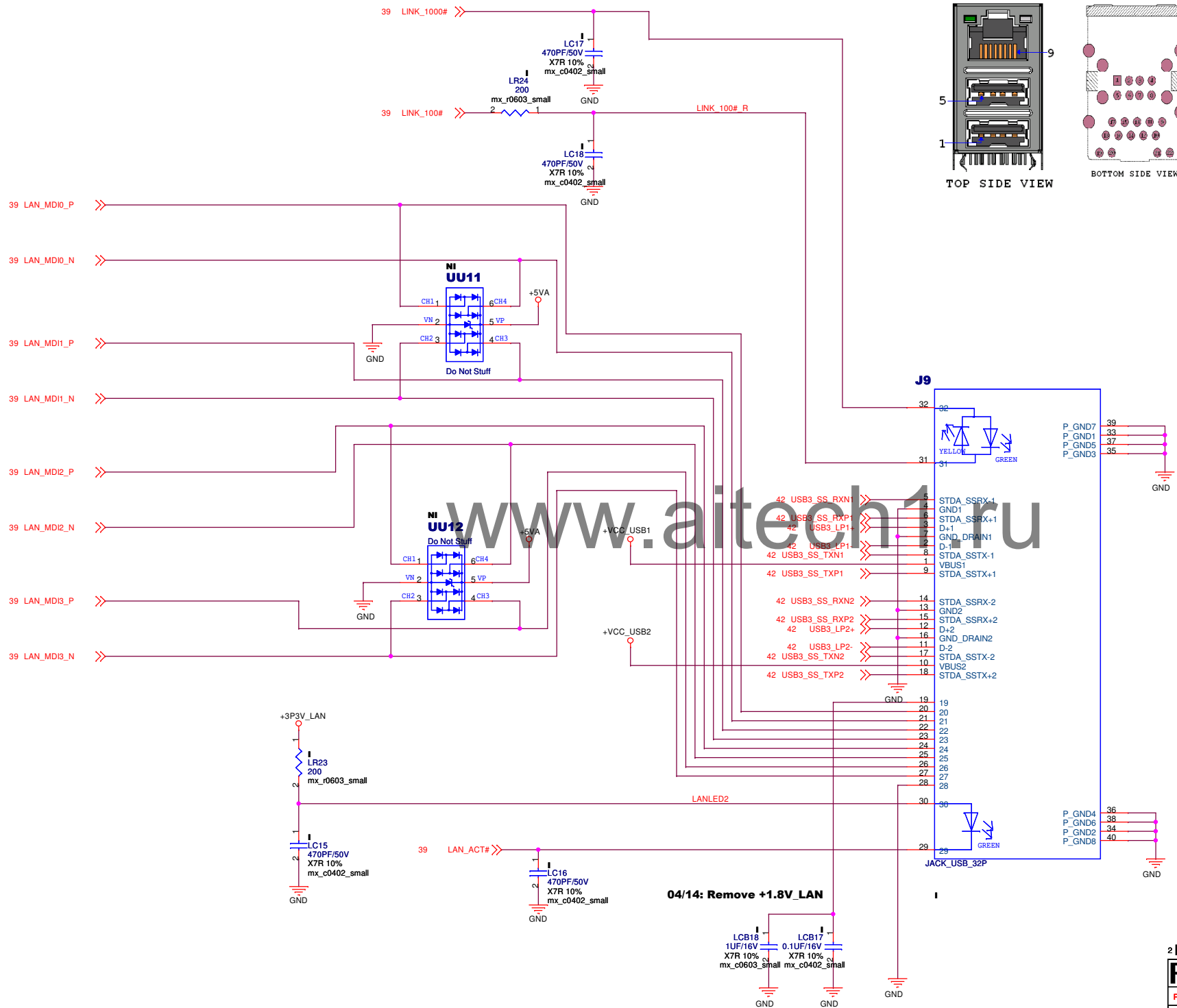
PEGATRON DT-MB RESTRICTED SECRET

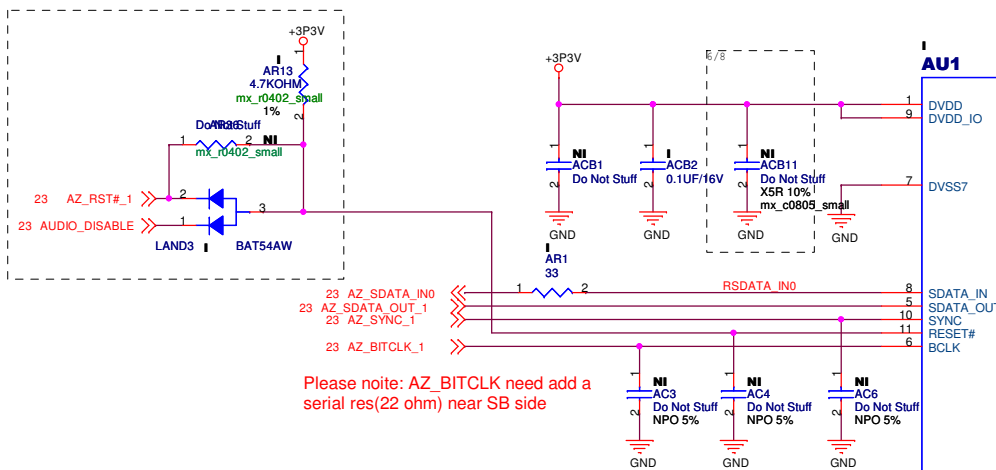
**PEGATRON** Title : RJ45+USB CONN 1

Pegatron Corp. Engineer: KJ Chang

Size	Project Name	Rev
A3	IPX61-DL	1.00

Date: Wednesday, September 29, 2010 Sheet 42 of 74



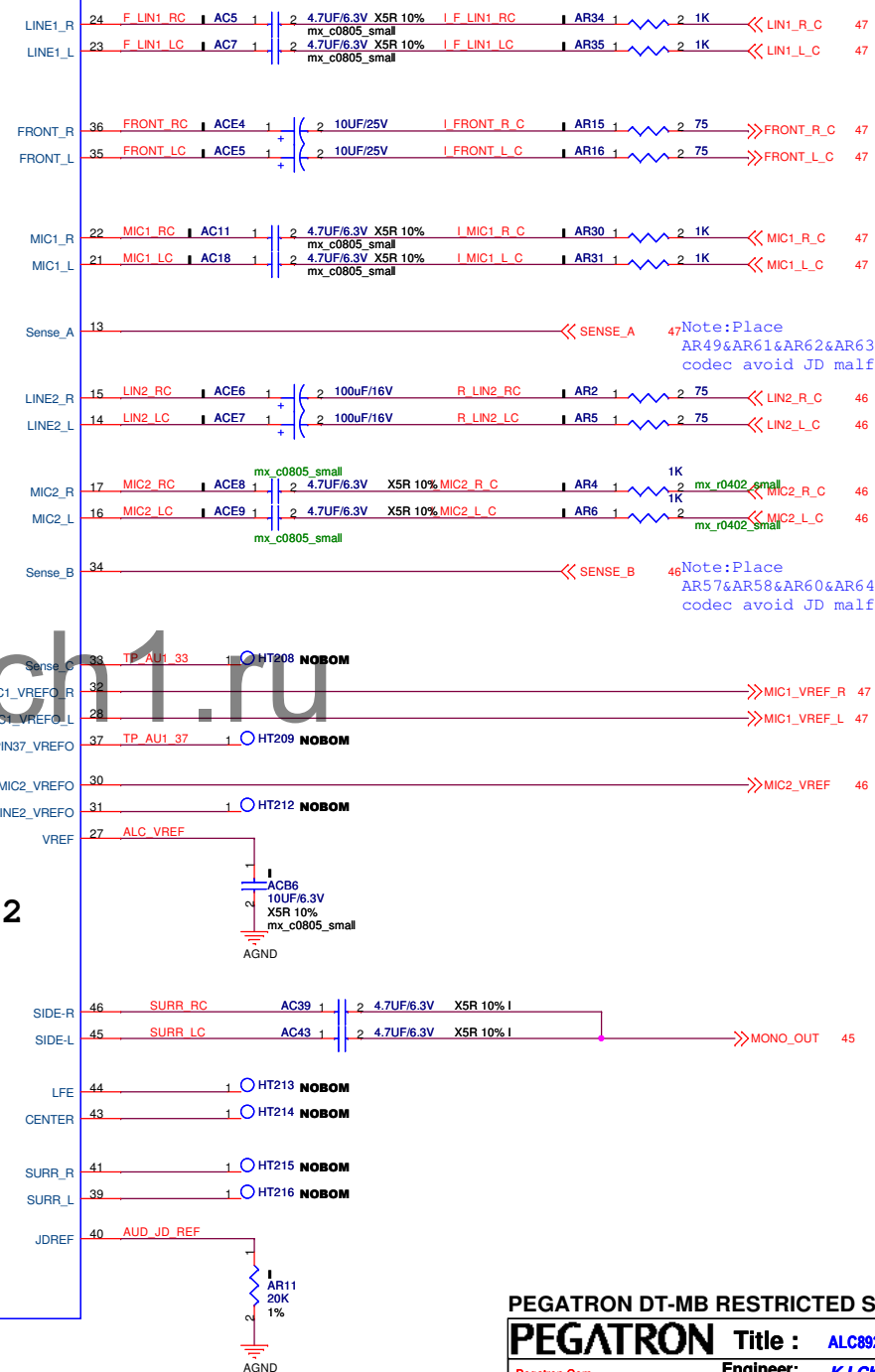


Change ACE864/ACE865/AC6 to 4.7uF/X5R/0805/10V because CD-IN are dedicated Input port , and for better noise immunity

If CD function not be used, please let CD-GND pin floating

If pin 23/24 and pin 21/22 support retasking function, please changed AR34/AR35/AR30/AR31 to 75 ohm

If front Microphone is not support retasking function, 1.ACE8/ACE9 can be changed to SMD 4.7uF(11X234475150) 2.please change AR4/AR6 to 1K for better ESD immunity

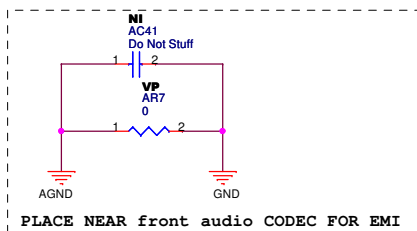


Note:Place AR49&AR61&AR62&AR63 near to codec avoid JD malfunction

Note:Place AR57&AR58&AR60&AR64 near to codec avoid JD malfunction

Need ESD DIODE?

ALC892



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : ALC892 CODEC

Engineer: KJ Chang

Size A3 Project Name IPX61-DL

Date: Wednesday, September 29, 2010 Sheet 44 of 74



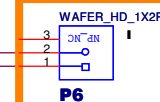
## Chassis Speaker Out Connector

**Note:**  
**For BPC Model Only Used**

12G080304020 => HR/A2502WV-2P <G>  
12G080300028 => FOXCONN/HD4502E-K <G>

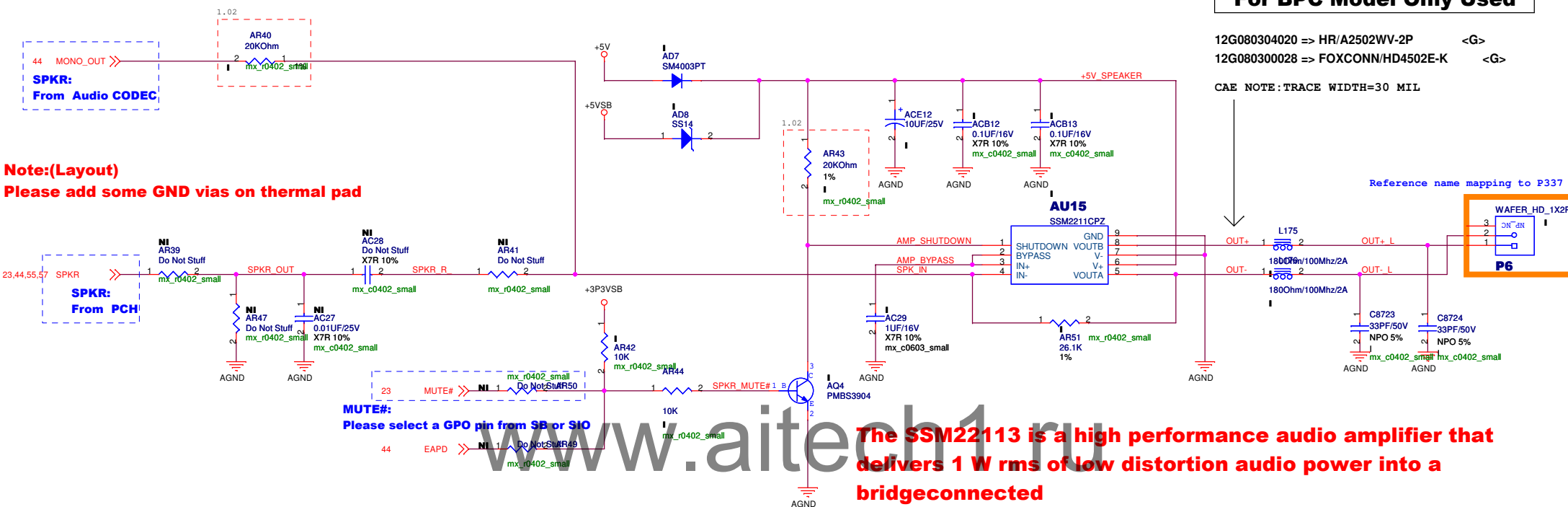
CAE NOTE: TRACE WIDTH=30 MIL

Reference name mapping to P337



P6

The SSM22113 is a high performance audio amplifier that delivers 1 W rms of low distortion audio power into a bridgeconnected 8  $\Omega$  speaker load (or 1.5 W rms into 4  $\Omega$  load).



**Note:(Layout)**  
**Please add some GND vias on thermal pad**

**MUTE#:**  
Please select a GPO pin from SB or SIO

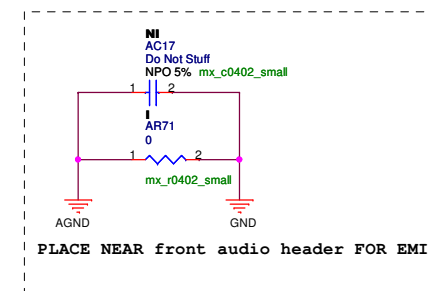
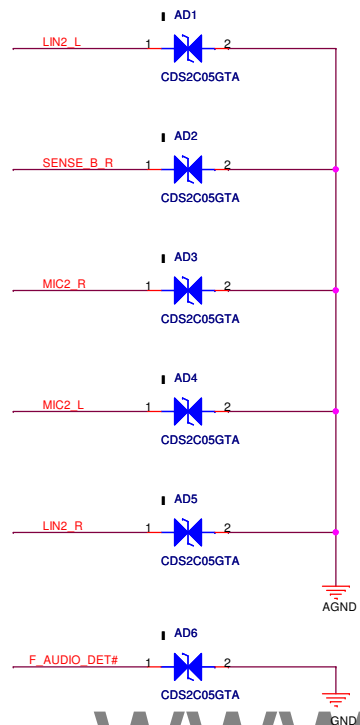
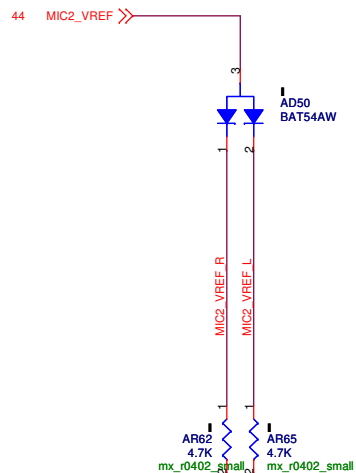
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **INTERNAL SPEAKER**

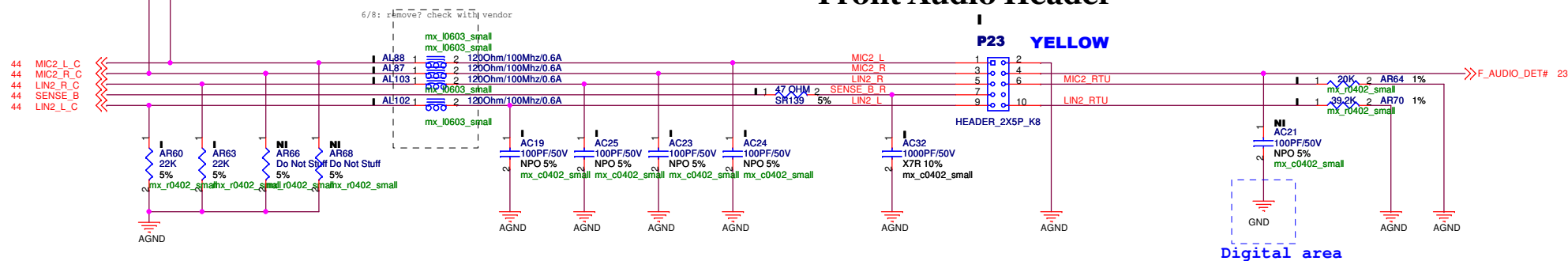
Pegatron Corp. Engineer: **KJ Chang**

Size A3 Project Name **IPX61-DL** Rev 1.00

Date: Wednesday, September 23, 2010 Sheet 45 of 74



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Front Audio Header



If ACE8/ACE9 use SMD capacitors,  
AR55/AR56 can be removed.

Digital area

AR57&AR58 Place near to codec  
for avoid JD malfunction

If front HP-OUT is not support retasking,  
these Vreference circuit can be removed.

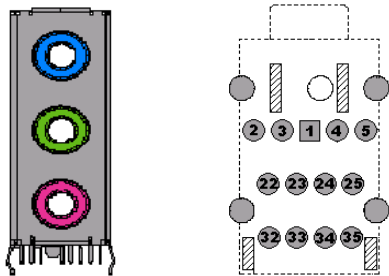
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : FROUT AUDIO CONN.

Pegatron Corp. Engineer: KJ Chang

Size A3 Project Name IPX61-DL Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 46 of 74

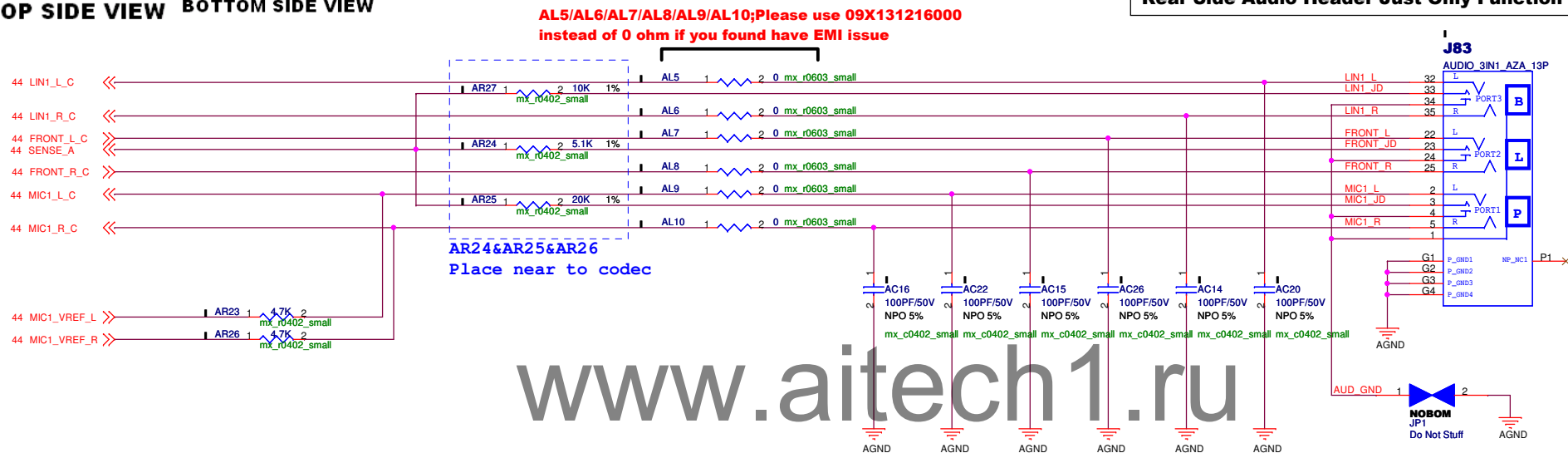


TOP SIDE VIEW BOTTOM SIDE VIEW

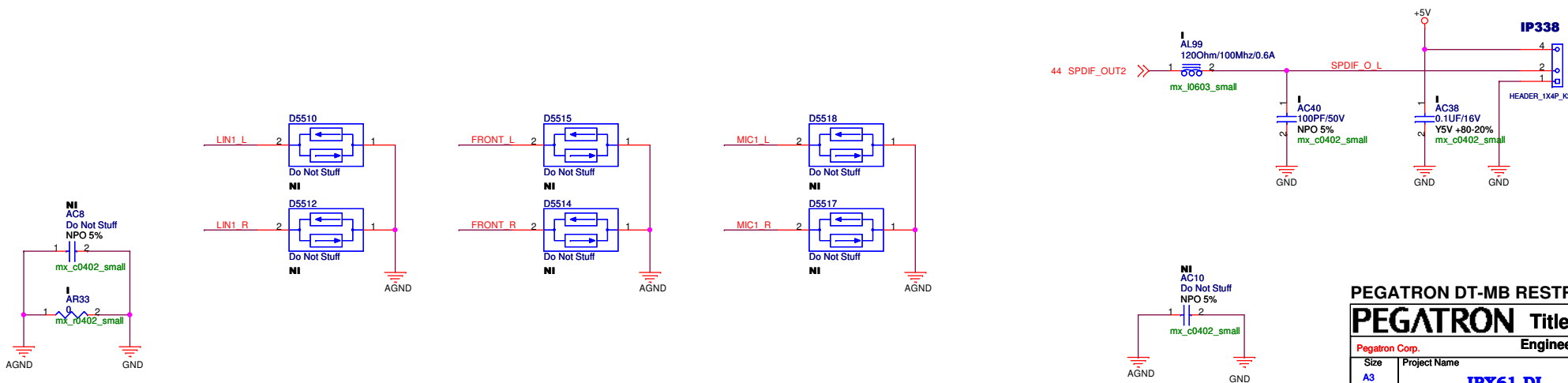
## Azalia Rear Audio Connector

### Note:

Rear Side Audio Header Just Only Function Dedicated



## SPDIF OUT2 CONNECTOR



PEGATRON DT-MB RESTRICTED SECRET

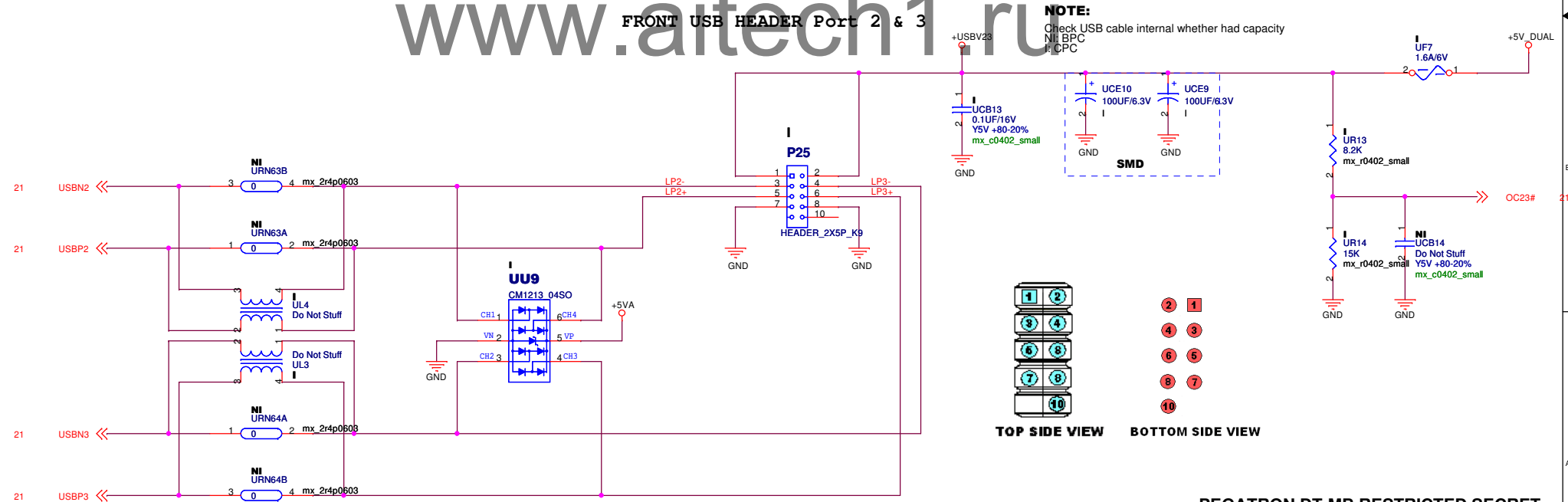
PEGATRON Title : AUDIO CONNECTOR 2/2

Pegatron Corp. Engineer: KJ Chang

Size A3 Project Name IPX61-DL Rev 1.00

Date: Wednesday, September 23, 2010 Sheet 47 of 74

FRONT USB HEADER Port 2 & 3



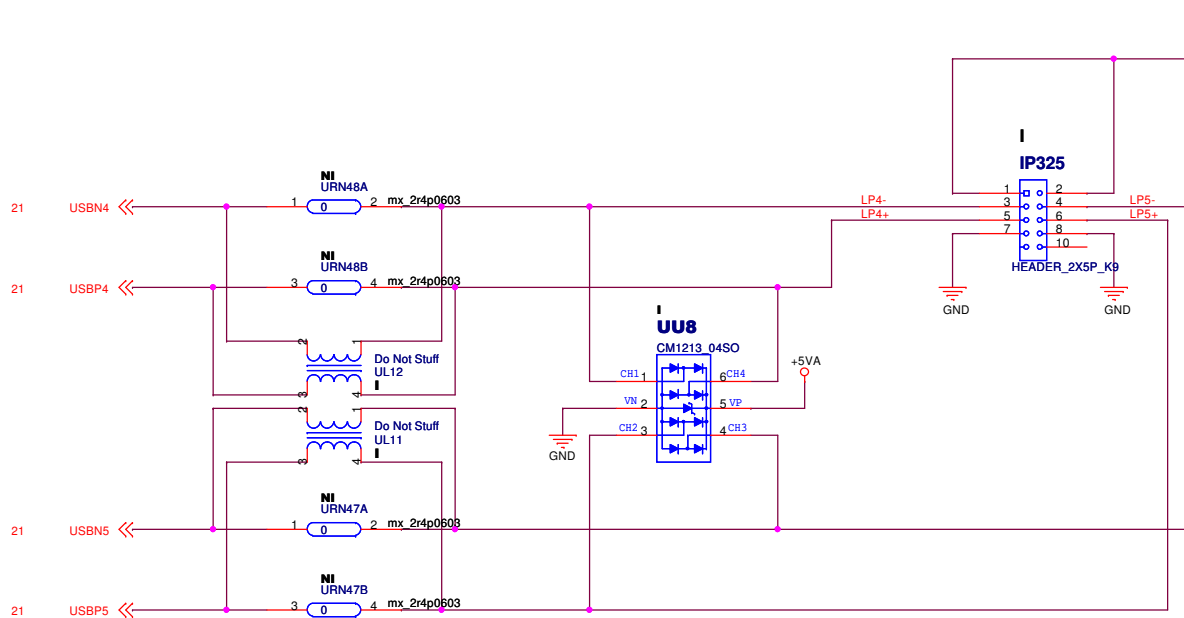
<b>PEGATRON DT-MB RESTRICTED SECRET</b>			
<b>PEGATRON</b>		<b>Title : USB HEADER - 1 and 2</b>	
<b>Pegatron Corp.</b>		<b>Engineer: <i>KJ Chang</i></b>	
Size <b>A3</b>	Project Name <b>IPX61-DL</b>	Rev <b>1.00</b>	
Date: <b>Wednesday, September 29, 2010</b>		Sheet <b>48</b> of <b>74</b>	

**NOTE:**  
Check USB cable internal whether had capacity  
NI: BPC  
I: CPC

**COMPONENTS:**  
+USBV45  
UCB17 0.1uF/16V Y5V +80-20% mx\_c0402\_small  
UCE8 100uF/6.3V SMD  
UCE14 100uF/6.3V SMD  
UR15 8.2K mx\_r0402\_small  
UR16 15K mx\_c0402\_small  
UCB18 Do Not Stuff Y5V +80-20% mx\_c0402\_small  
UF8 1.6A/6V  
+5V\_DUAL  
OC45# 21

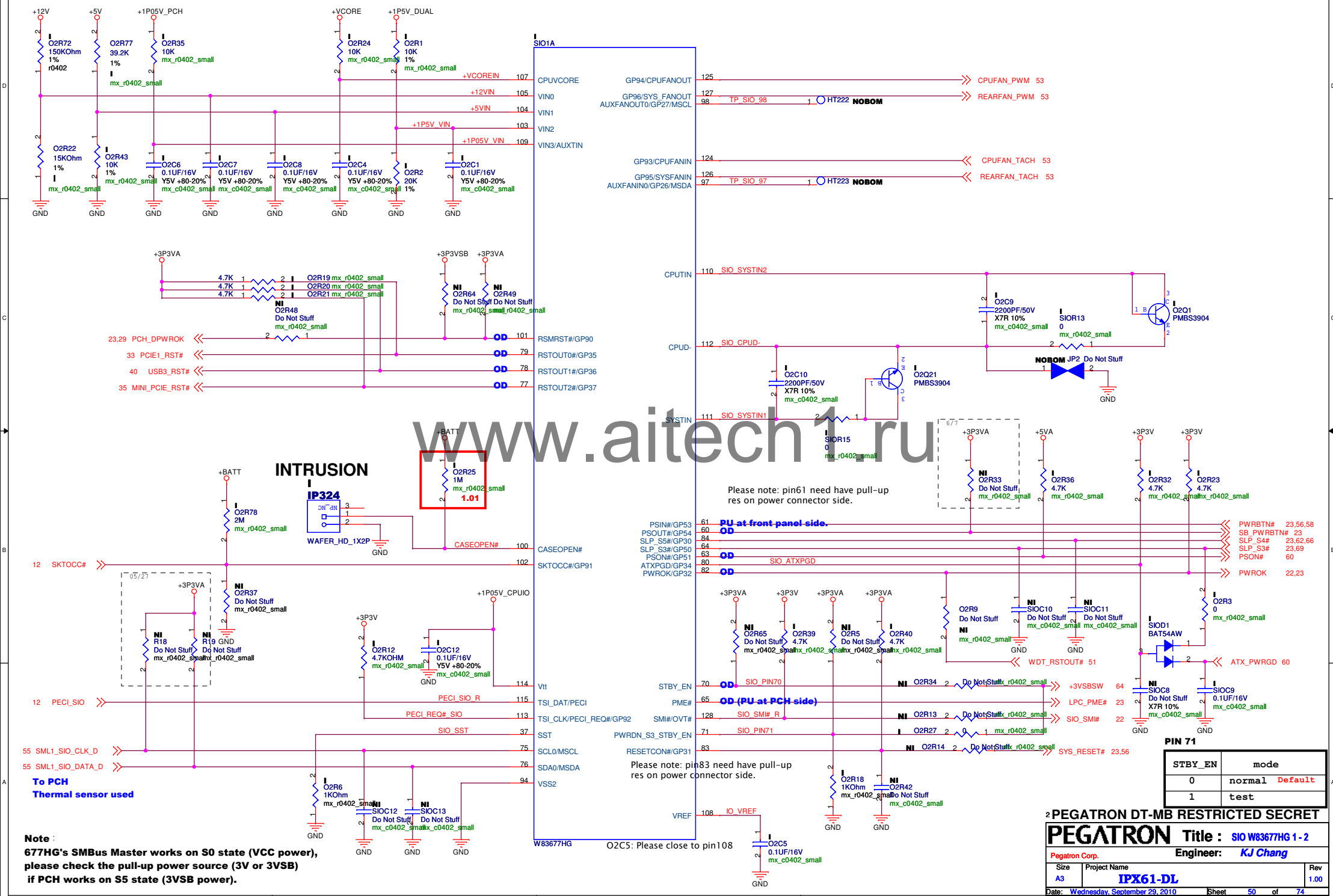
**BOTTOM SIDE VIEW**  
2 1  
4 3  
6 5  
8 7  
10

**TOP SIDE VIEW**  
1 2  
3 4  
5 6  
7 8  
9 10



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**Please do not leave pin 103 VCORE\_REFIN floating.  
Otherwise, pin 63 PSON# will be affected and the system cannot be booted.**



**NOTE :**  
**PIN51/52/54/55 is OD PIN**  
**Please check if another side**  
**already Pull-up**

NOBOM	ST188	1	TP SIO PIN6	6
NOBOM	ST215	1	TP SIO PIN11	11
NOBOM	ST216	1	TP SIO PIN12	12
NOBOM	ST217	1	TP SIO PIN13	13
NOBOM	ST218	1	TP SIO PIN5	38
NOBOM	ST189	1	TP SIO PIN6	95
NOBOM	ST130	1	TP SIO PIN3	3
NOBOM	ST131	1	TP SIO PIN4	4
NOBOM	ST132	1	TP SIO PIN5	5
NOBOM	ST133	1	TP SIO PIN7	7
NOBOM	ST134	1	TP SIO PIN8	8
NOBOM	ST135	1	TP SIO PIN9	9
NOBOM	ST136	1	TP SIO PIN10	10
NOBOM	ST137	1	TP SIO PIN14	14

31	XINIT#	52
31	XSLIN#	51
31	XAFD#	54
31	XSTB#	55
31	ACK#	41
31	PE BUSY	39
31	PE BUSY	40
31	XPD7	42
31	XPD6	43
31	XPD5	44
31	XPD4	45
31	XPD3	46
31	XPD2	47
31	XPD1	48
31	XPD0	49
31	XPD0	50

DIR#/GP03/CIRT2	52
WP#/CIR BLTX1_Sense/GP55	51
RODATA#/CIR BLTX2_Sense/GP56	54
HEAD#/CIRLED/GP57	55
CIRRXWB/SLCT/GP97	41
GP24/CIRRX	53
GP25/CIRTX	39
INDEX#/AUX_FANIN1	40
MOA#/GP01	42
DSA#/GP02	43
STEP#/HD_LED#	44
WD#/GP04	45
WE#/GP05	46
TRAK0#/PRIMARY_HD#	47
DSKCHG#/SECONDARY_HD#	48

SCL2/MSCL/GP83/INIT#	23
SDA2/MSDA/GP84/SLIN#	22
SDA1/GP81/AFD#	21
SCL1/GP80/STB#	20
DGLW/GP85/ACK#	25
DAC_RST#/GP82/ERR#	18
YLW_LED/GP87/PE	17
GRN_LED/GP86/BUSY	19
DGH#/GP47/PD7	26
LED_G/GP46/PD6	25
LED_F/GP45/PD5	24
LED_F/GP44/PD4	23
LED_D/GP43/PD3	22
LED_C/GP42/PD2	21
LED_B/GP41/PD1	20
LED_A/GP40/PD0	25

VID0/GP70/BUSSEL1_1	83
VID01/GP71/BUSSEL2_1	92
VID02/GP72/BUSSEL3_1	91
VID03/GP73/BUSSEL1_0	90
VID04/GP74/BUSSEL2_0	89
VID05/GP75/BUSSEL3_0	88
VID06/GP76	87
VID07/GP77	86
GP10/VID10	123
GP11/VID11	122
GP12/VID12	121
GP13/VID13	120
GP14/VID14	119
GP15/VID15	118
GP16/VID16	117
GP17/VID17	116

GP52(PORT80_EN)	62
GP33(PGD100)	81
WDT_RSTOUT#	72
EN_DACOUT	74
VID_DAC	66
DAC_V3	67
DAC_V2	68
DAC_V1	69
GP63(SINA)	33
(FAN_SET)GP62/SOUTA	34
GP66/DSRA#	30
(2E_4E_SEL)GP65/RTSA#	31
GP67/CTS#	29
(BUSSEL_EN)GP64/DTRA#	32
GP60/RIA#	36
GP61/DCDA#	35

**PORT80\_EN(PIN62)**

PORT80_EN	FUNCTION
0	GPIO
1	PIN 38~45, 47~55 function selection
Default	

**PWROK signal deley selection (PIN 81)**

PGD100	PWROK DELEY
0	0 ms
1	100 ms
Default	

**EN\_DACOUT (PIN 74)**

EN_DACOUT	DAC OUTPUT
0	Disable
1	Enable
Default	

**LPC address selection (PIN 31)**

RTSA#	CONFIG PORT ADDR
0	0x002E Default
1	0x004E

**BUSSEL function enable/disable (PIN32)**

DTR1#	BUSSEL_EN	PIN.88~93
0	DISABLE	VIDO
1	ENABLE	BUSSEL IN/OUT

**Fan initial speed selection(PIN34)**

TXD1	FANSET
0	50% Default
1	100%

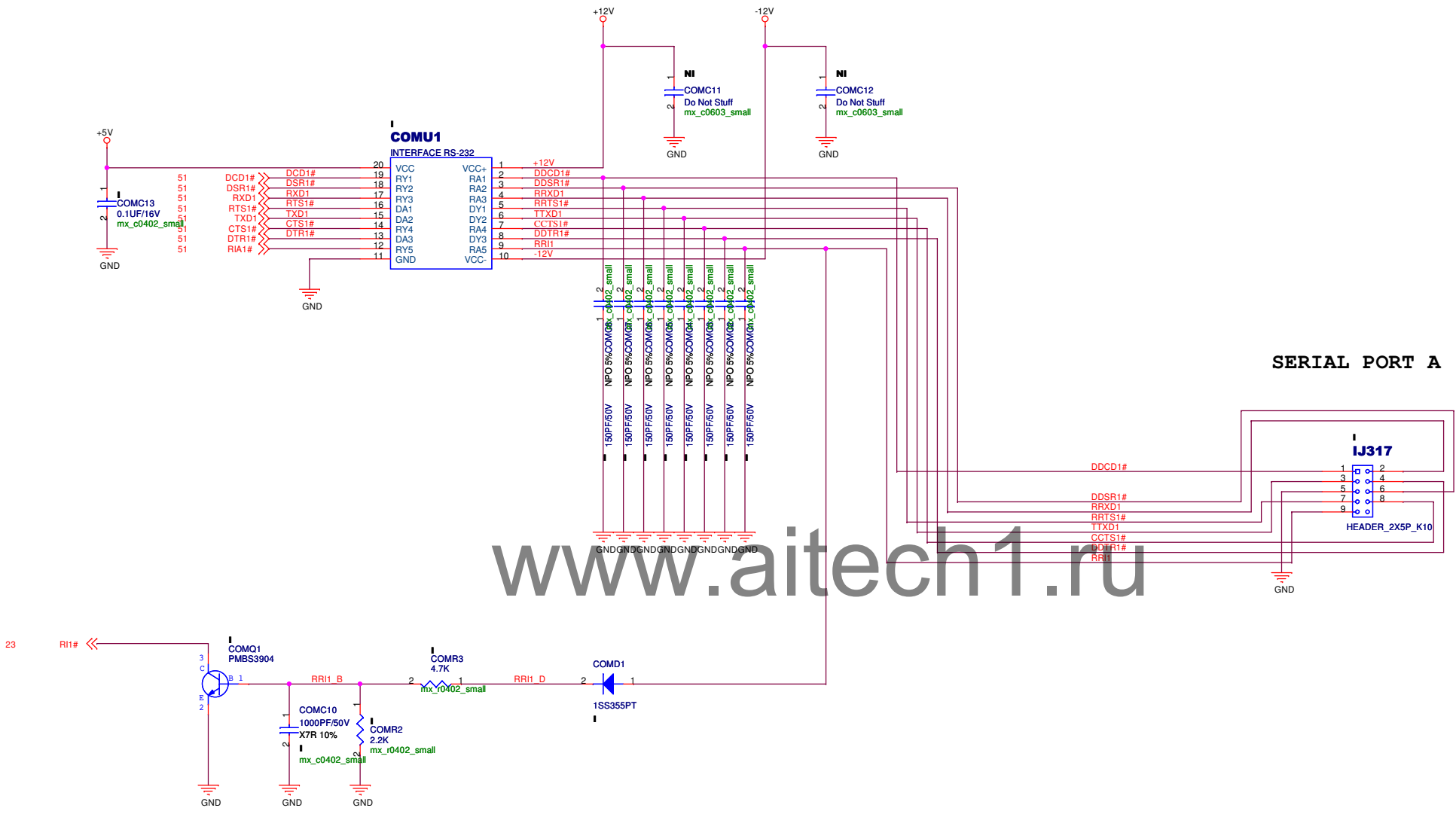
**PIN73 :**  
**If we want to use 3VSBSW function, please pull up to 3VSB with 4.7Kohm**  
**Otherwise pull down RSVD with 4.7Kohm, then pin70 is STBY\_EN function.**

**PEGATRON DT-MB RESTRICTED SECRET**

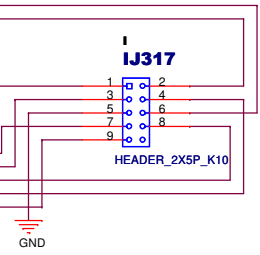
**PEGATRON** Title : **SIO W83677HG 2.2**

Pegatron Corp. Engineer: **KJ Chang**

Size A3	Project Name <b>IPX61-DL</b>	Rev 1.00
Date: Wednesday, September 29, 2010	Sheet 51 of 74	



**SERIAL PORT A**

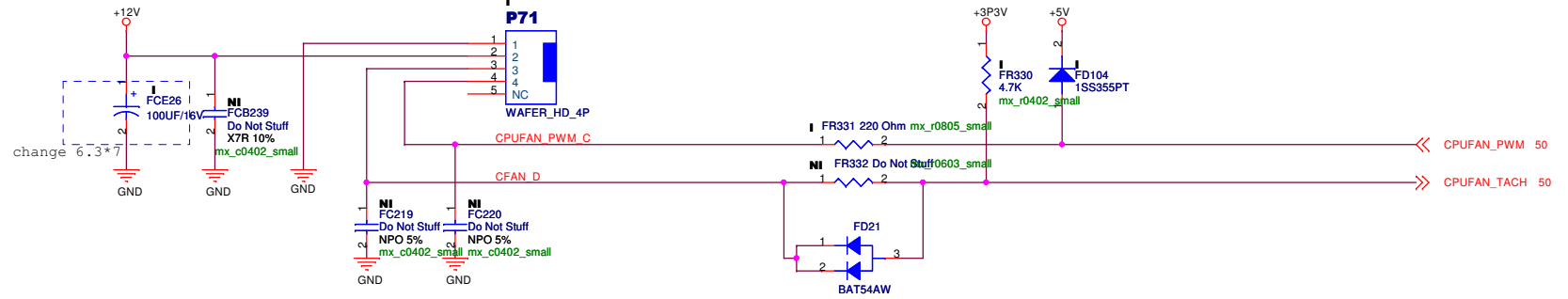




# CPU FAN

COLOR: WHITE

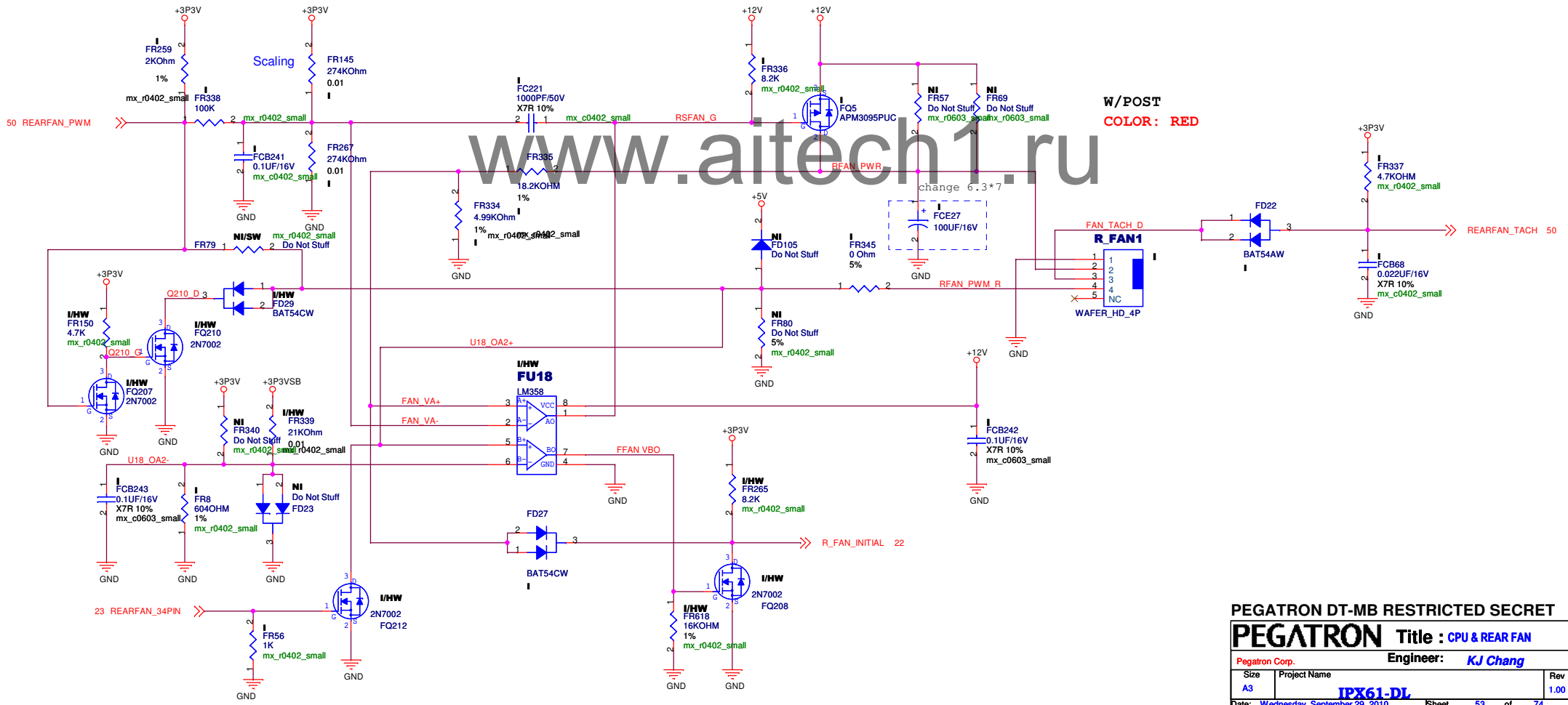
W/POST



# REAR FAN

COLOR: RED

W/POST



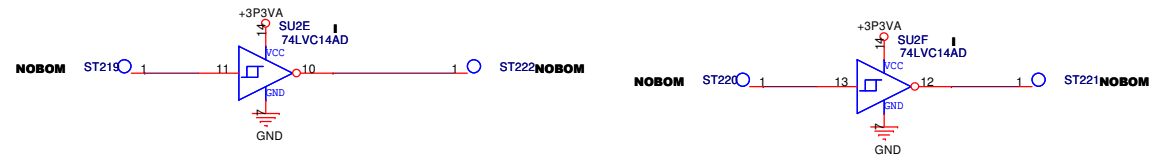
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : CPU & REAR FAN

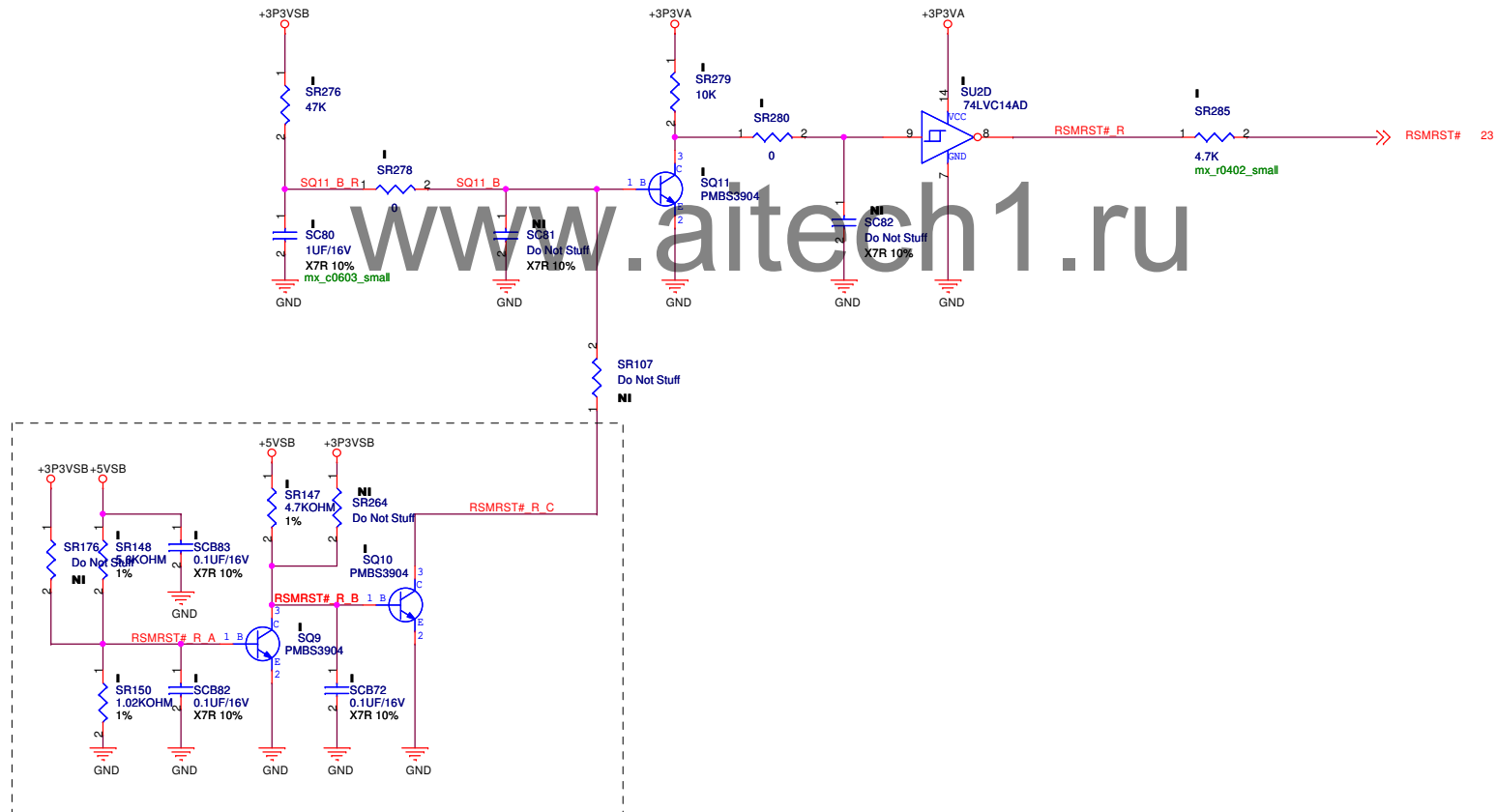
Engineer: KJ Chang

Size A3 Project Name IPX61-DL

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# 05/31: External RSMRST#



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **RSMRST#**

Pegatron Corp.

Engineer: **KJ Chang**

Size	Project Name	Rev
A3	<b>IPX61-DL</b>	1.00

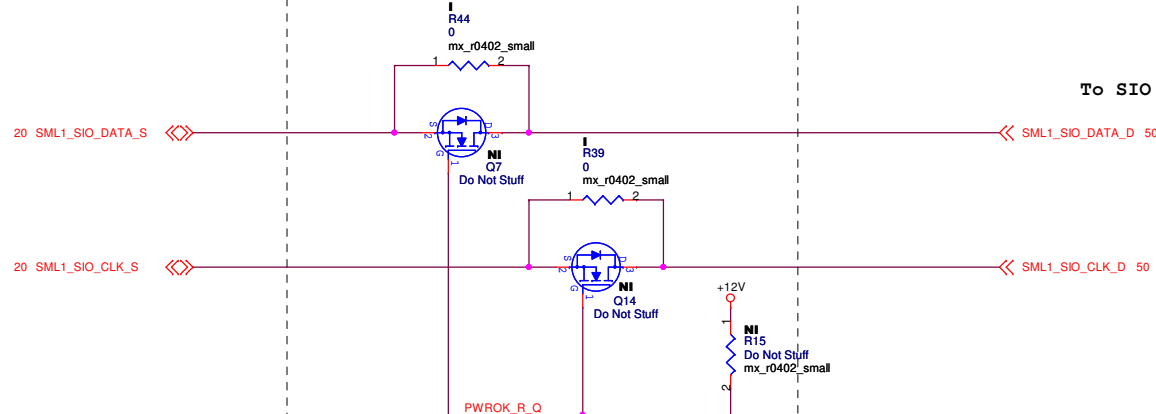
Date: Wednesday, September 29, 2010 Sheet 54 of 74

# SM BUS Control

05/27

To PCH

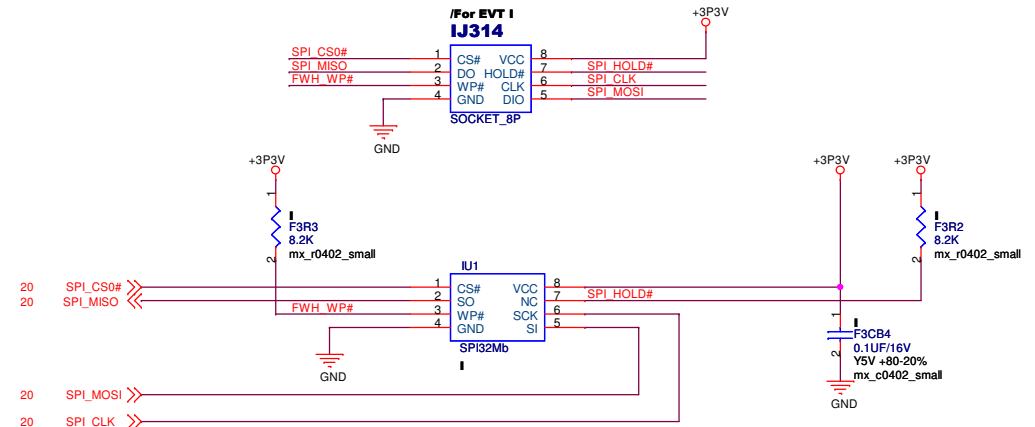
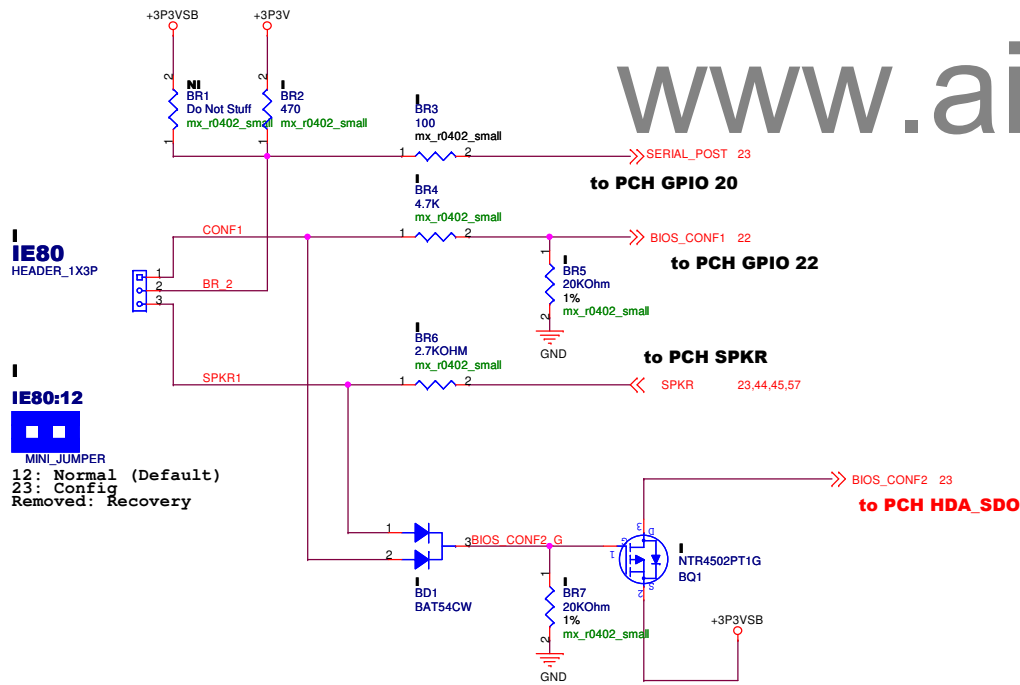
To SIO



## BIOS CONFIGURATION

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SPI BIOS ROM - 4 MB



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **SM BUS & SPI ROM**

Pegatron Corp. Engineer: **KJ Chang**

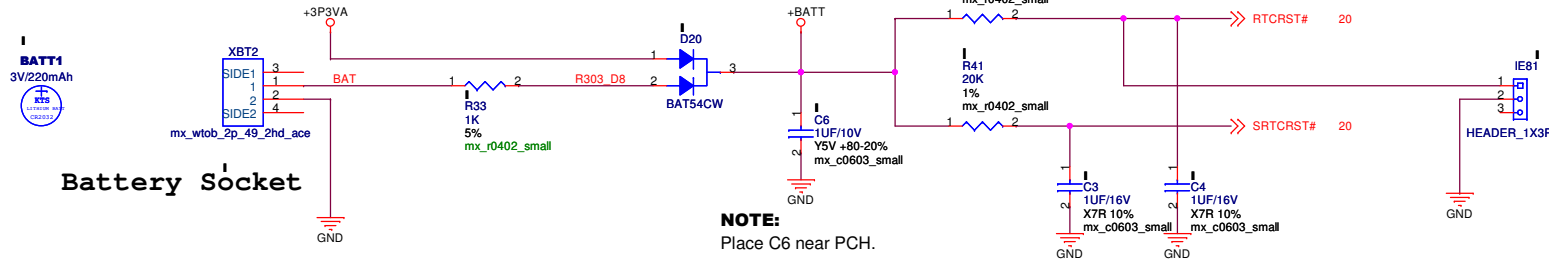
Size A3 Project Name **IPX61-DL** Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 55 of 74

PWRBTN# of PCH is internally pulled-up in PCH to 3.3 V standby through a weak pull-up 24Kohm.

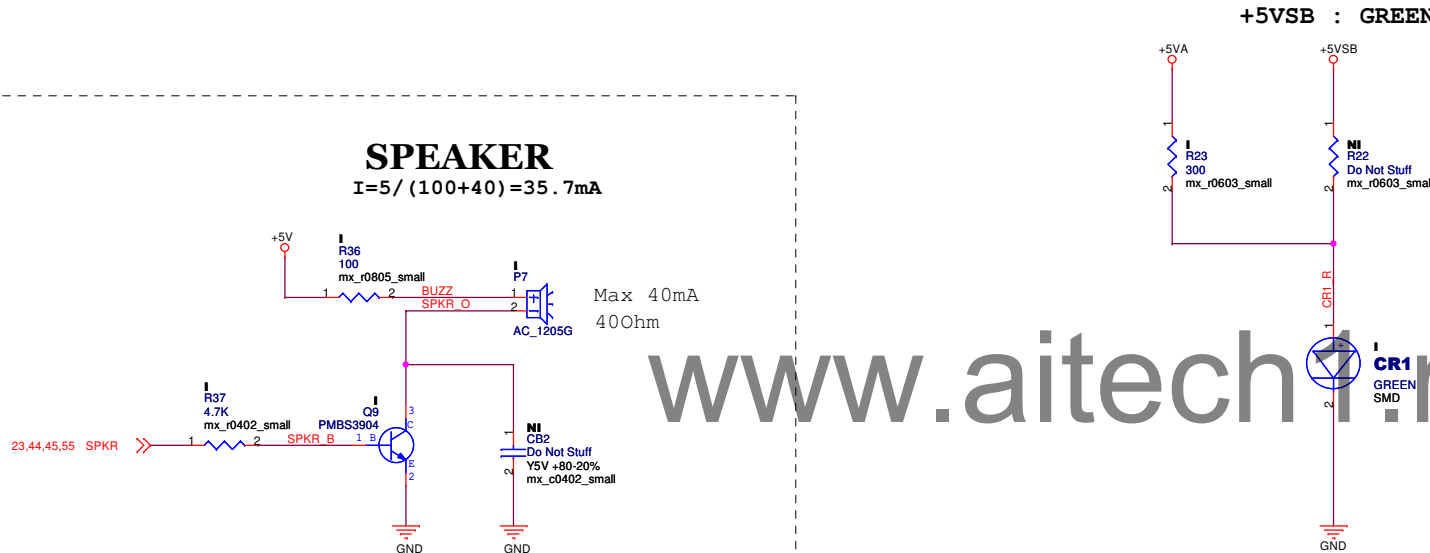


# External RTC Circuitry



## SPEAKER

$$I = 5 / (100 + 40) = 35.7 \text{ mA}$$

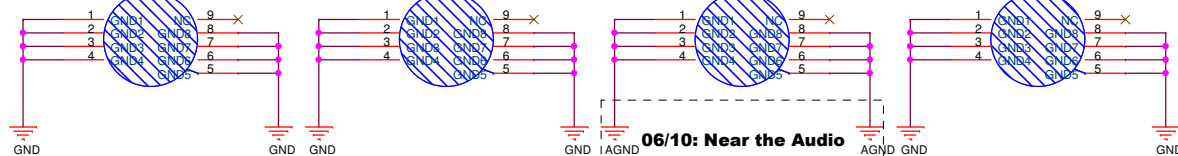


**NOBOM**  
H1  
Do Not Stuff

**NOBOM**  
H2  
SCREW HOLE\_160\_HP

**NOBOM**  
H3  
Do Not Stuff

**NOBOM**  
H4  
Do Not Stuff



**ONLY FOR INTEL SCREW HOLE**

**LB1**

1.375X0.25  
WHITE  
1D375XD025\_WHITE

**LB2**

1.0X0.187  
WHITE  
1D0X0D187\_WHITE

AA# : 1510-03MQ0IN (S : 1510-03MR0IN )

Product code : 1510-06DE0IN

2 PEGATRON DT-MB RESTRICTED SECRET

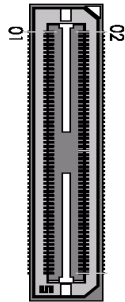
**PEGATRON** Title : RTC/COMS/SPKR/SCREW

Pegatron Corp. Engineer: **KJ Chang**

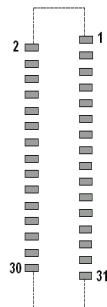
Size A3 Project Name **IPX61-DL** Rev 1.00

Date: Wednesday, September 29, 2010 Sheet 57 of 74

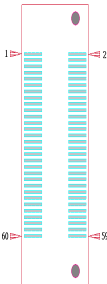




TOP SIDE VIEW



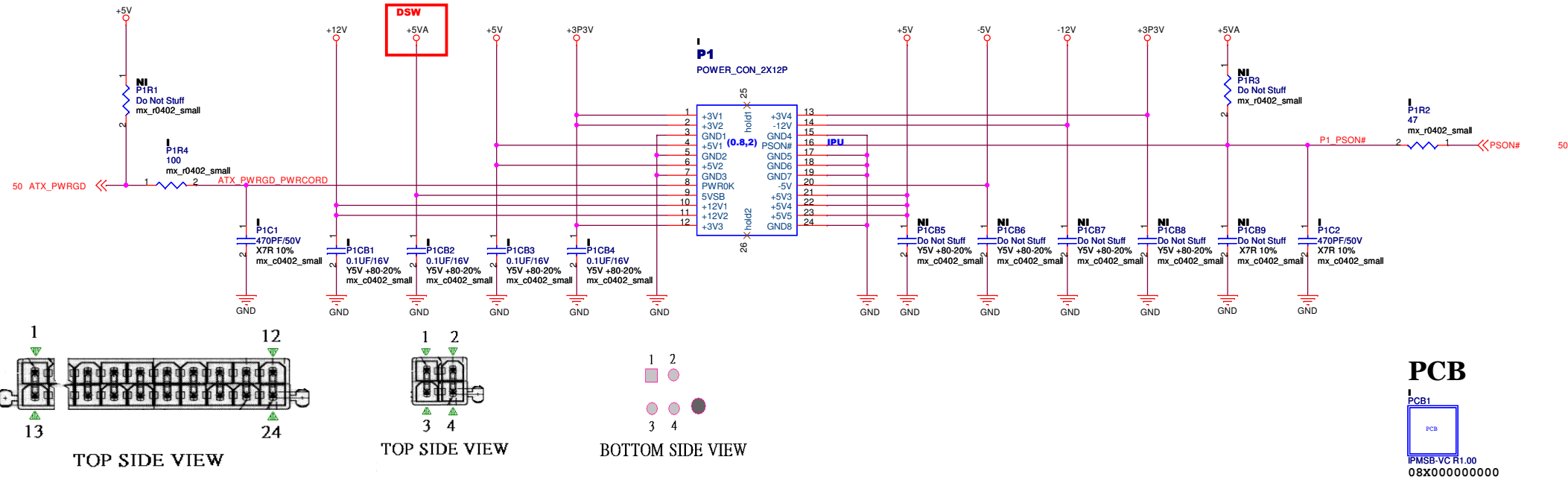
HRS/DF9C-31S-1V(22)  
PCB FOOTPRINT



BOTTOM SIDE VIEW

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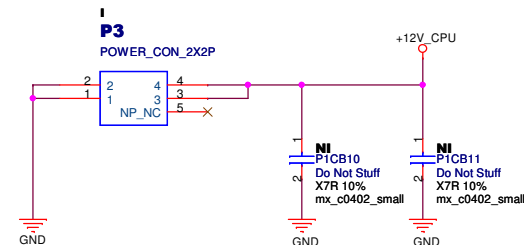
# ATX POWER\_24P SUPPLY CONNECTOR



Nodes related to different power planes

Node	Goal Q'ty
+5V	5
+5VSB	5
+12V	5
-12V	5
+3V	5
+Vcore	10
+GND	15
+12V_CPU	10

## VRM POWER\_4P SUPPLY CONNECTOR



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **ATX POWER\_24P**

Pegatron Corp. Engineer: **KJ Chang**

Size A3 Project Name **IPX61-DL** Rev 1.00

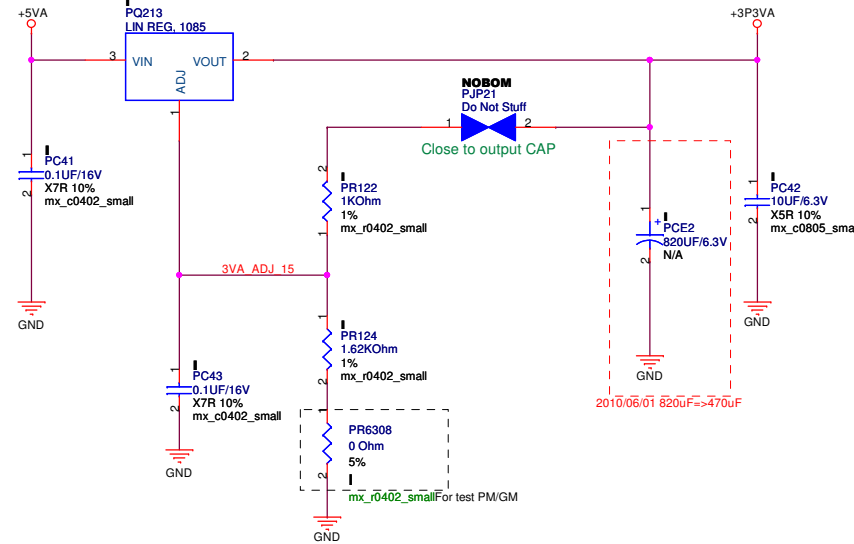
Date: Wednesday, September 29, 2010 Sheet 60 of 74



# +3P3VA

Itdc=2A I<sub>max</sub> = 3A

REG 1085 I<sub>max</sub>=3A



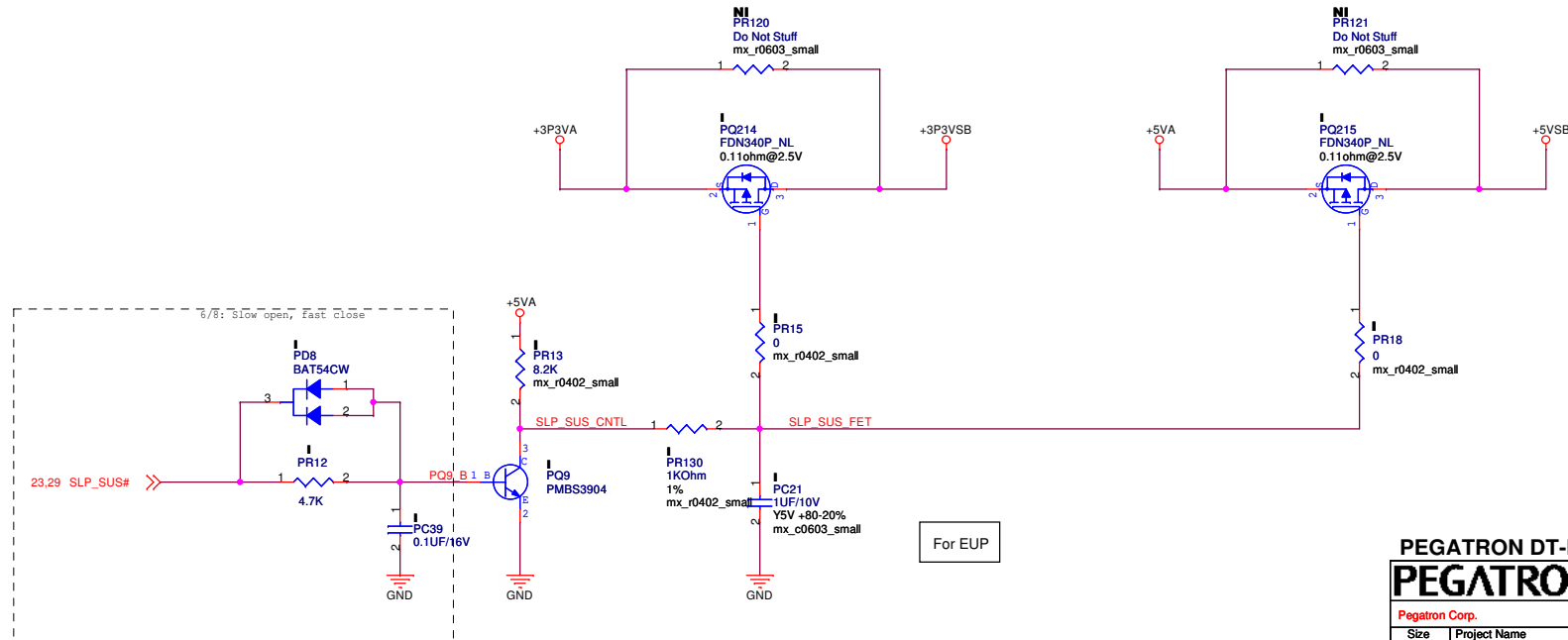
Vdroop1=I\*t/C=2.5\*4u/820u=0.012195V  
Vdroop2=2.5\*36m=0.09V  
Vdroop=0.102195V

VFB = 1.25V  
Vout = 1.25/1\*(1+1.62)+55uA\*1.62K = 3.3641 V

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+3P3VA => +3VSB

+5VA => +5VSB



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : +3VA&+3VSB&+5VSB

Pegatron Corp. Engineer: KJ Chang

Size	Project Name	Rev
A3	IPX61-DL	1.00

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		1			

V\_SM\_VTT<sub>30</sub>: Vddq/2 (1.0A TDC)

70 VRM\_PWRGD\_1V05

+5VSB

NI PR276 10K

NI PQ12 PMBS3904

NI PQ11 2N7002

NI PC220 0.1UF/16V X7R 10% mx\_c0603\_small

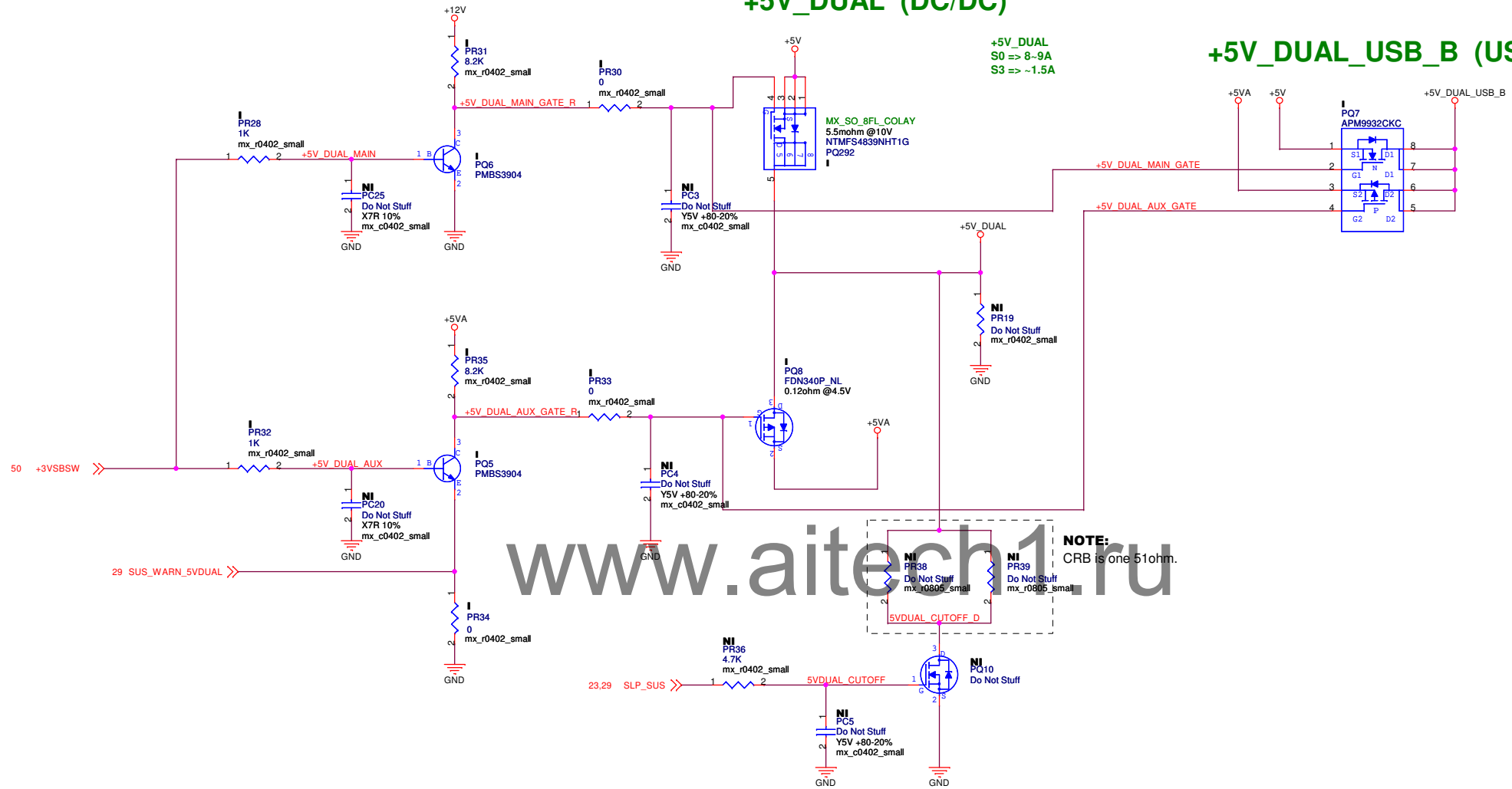
level ~ 1V  
 $I_c = (1-0.7)/10\text{kohm} \cdot 175 = 5.1\text{mA}$   
 $V_{ce} = 5 \cdot 10^{-3} \cdot 5.1 = -45\text{V(sat.)}$

VRM\_PWRGD 23,58,70,72

# **+5V\_DUAL (DC/DC)**

+5V\_DUAL  
S0 => 8~9A  
S3 => ~1.5A

# **+5V\_DUAL\_USB\_B (USB 2.0)**



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NOTE:  
CRB is one 51ohm.

PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **+5V\_DUAL**

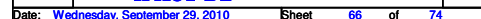
Pegatron Corp. Engineer: **KJ Chang**

Size A3 Project Name **IPX61-DL** Rev 1.00

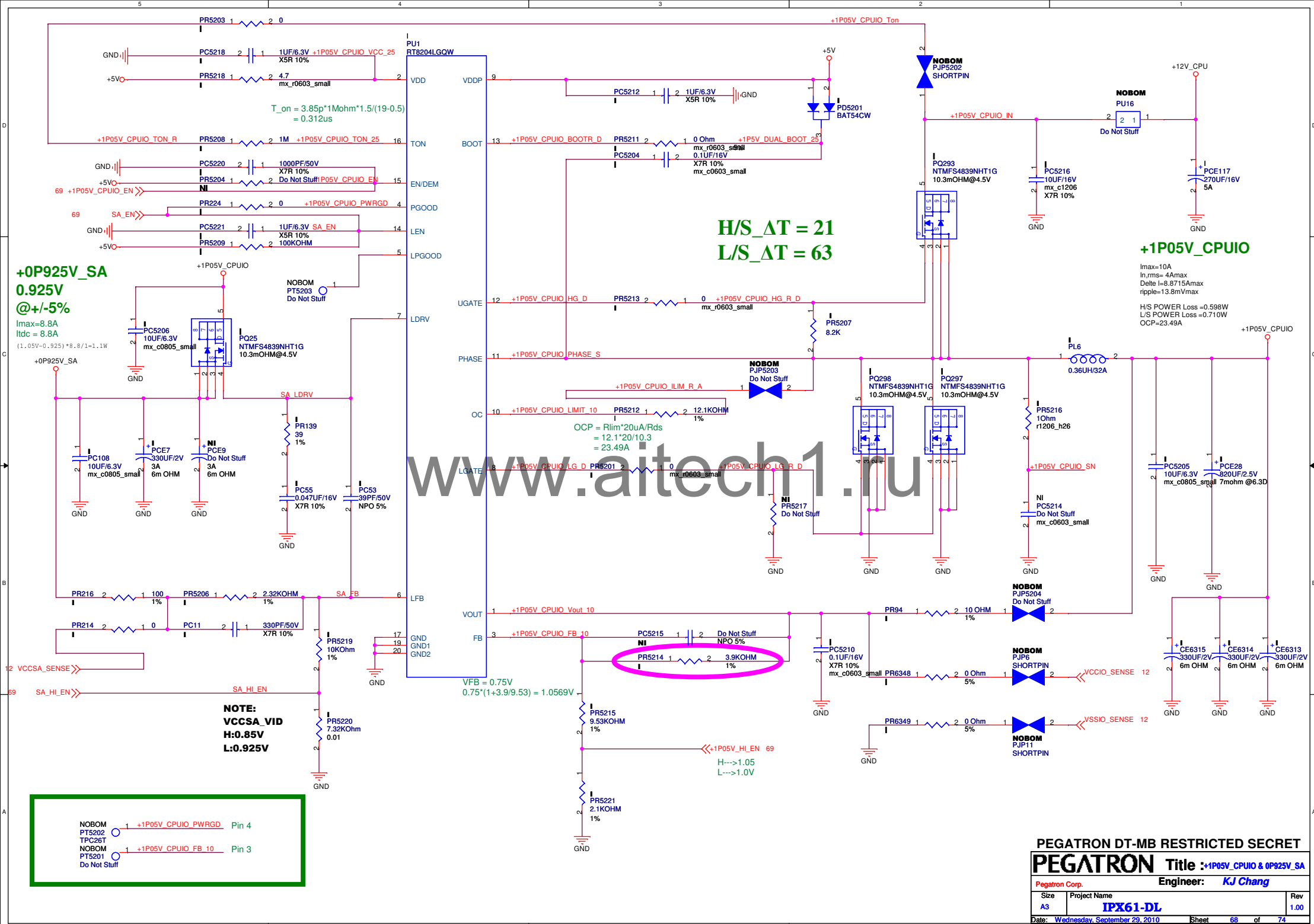
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Vin=5V  
Vout = 1P05V  
Imax:0.7A  
 $V_{droop} = 1.05 \cdot 0.7 \cdot 40 / 1000 = 1.022V$

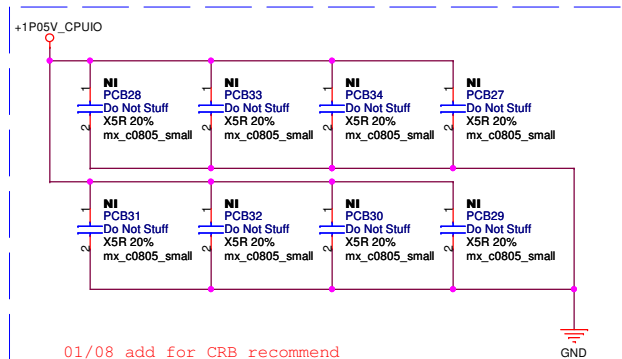
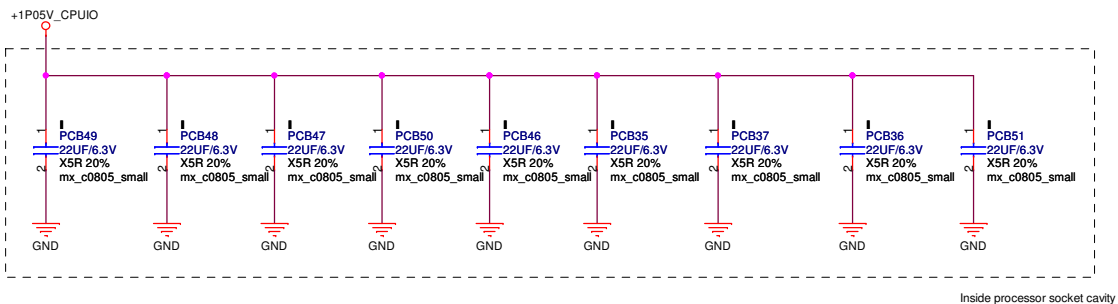


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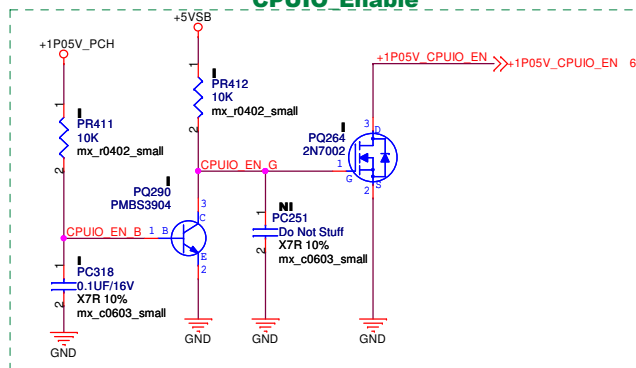




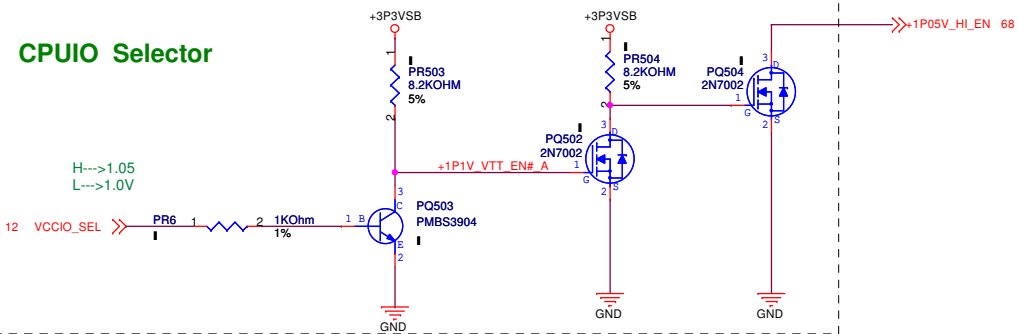
## +1P05V\_CPUIO Output MLCC



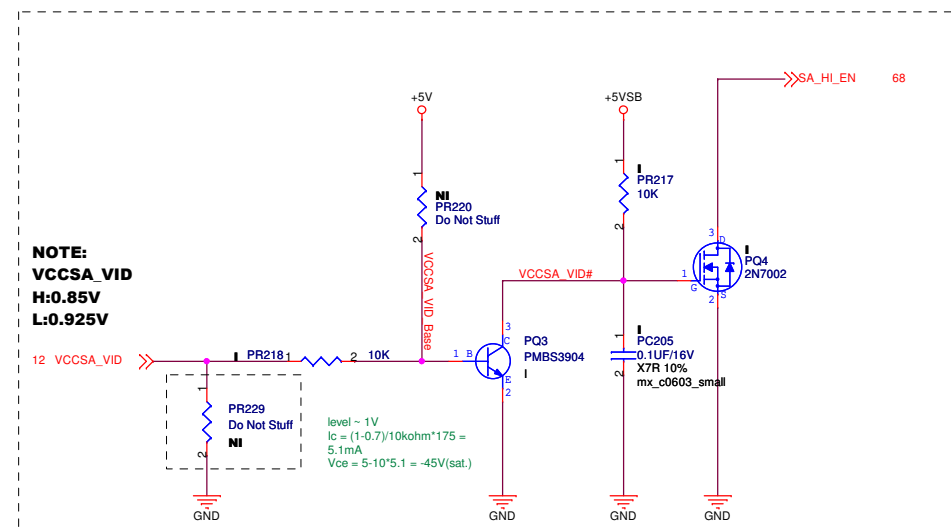
## CPUIO Enable



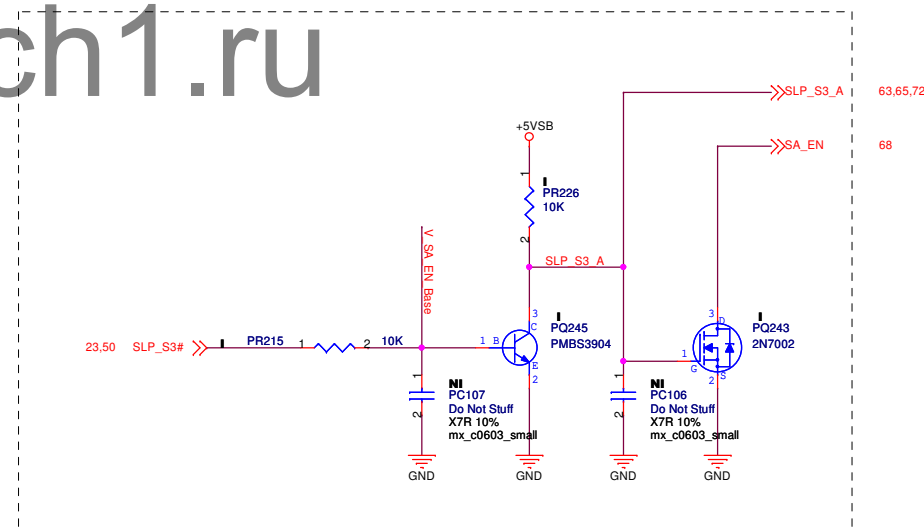
## CPUIO Selector



## +0P925V\_SA Selector



## +0P925V\_SA Enable



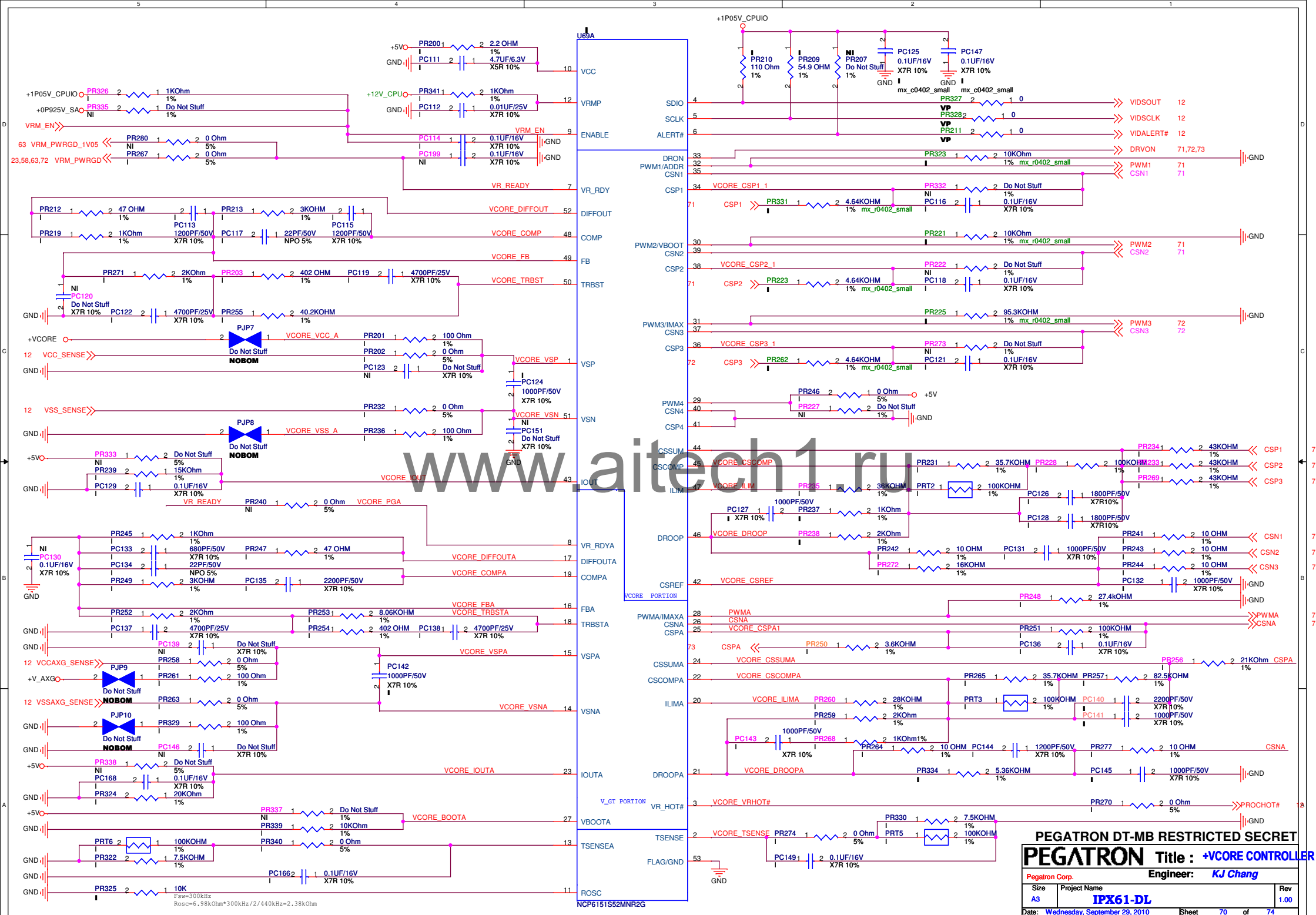
PEGATRON DT-MB RESTRICTED SECRET

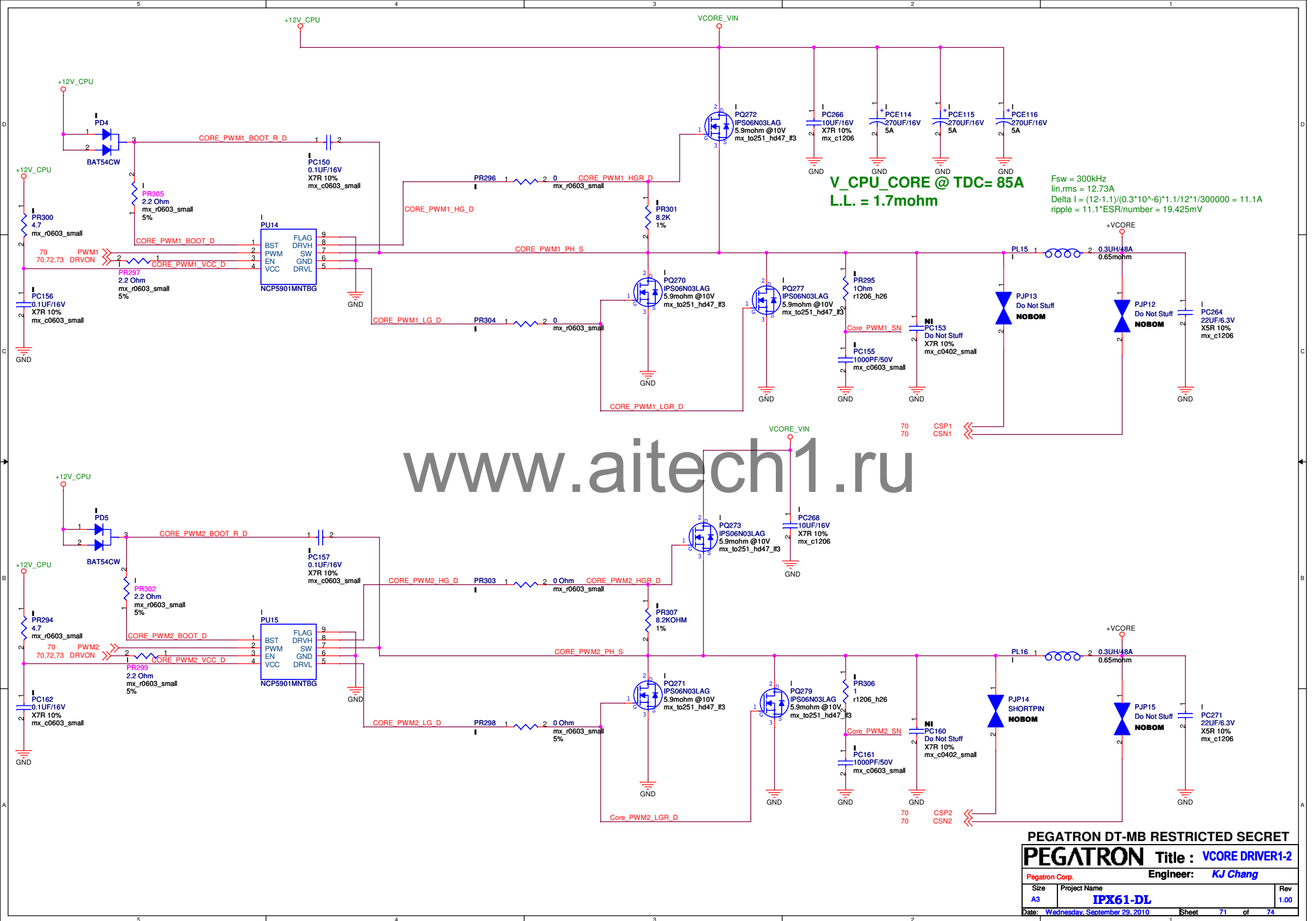
**PEGATRON** Title : 1P05V\_CPUIO DRIVER

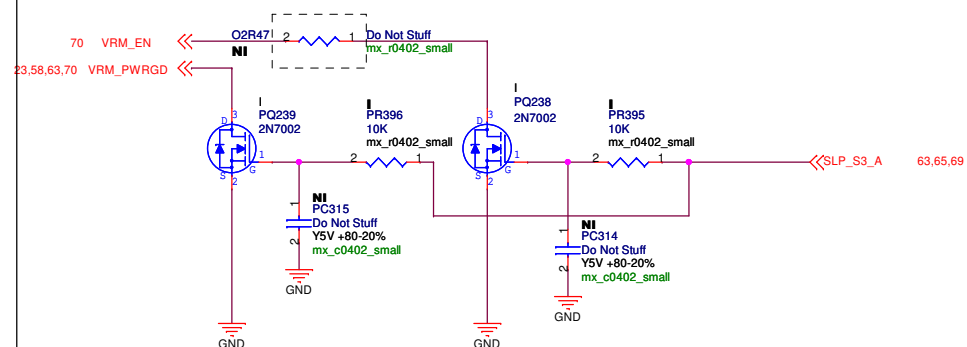
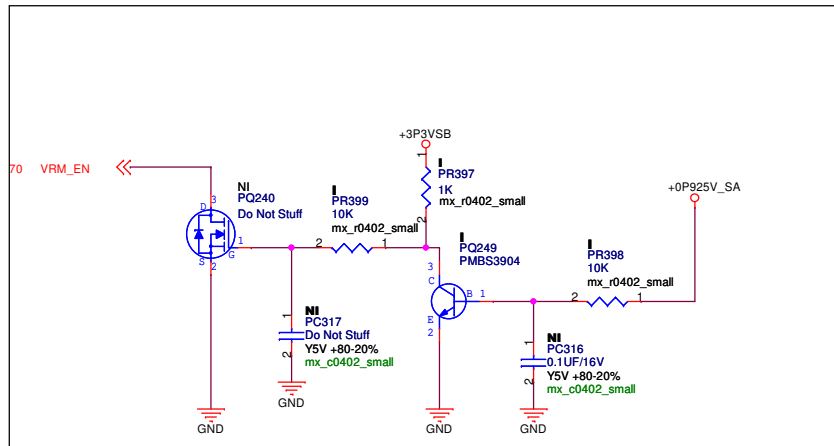
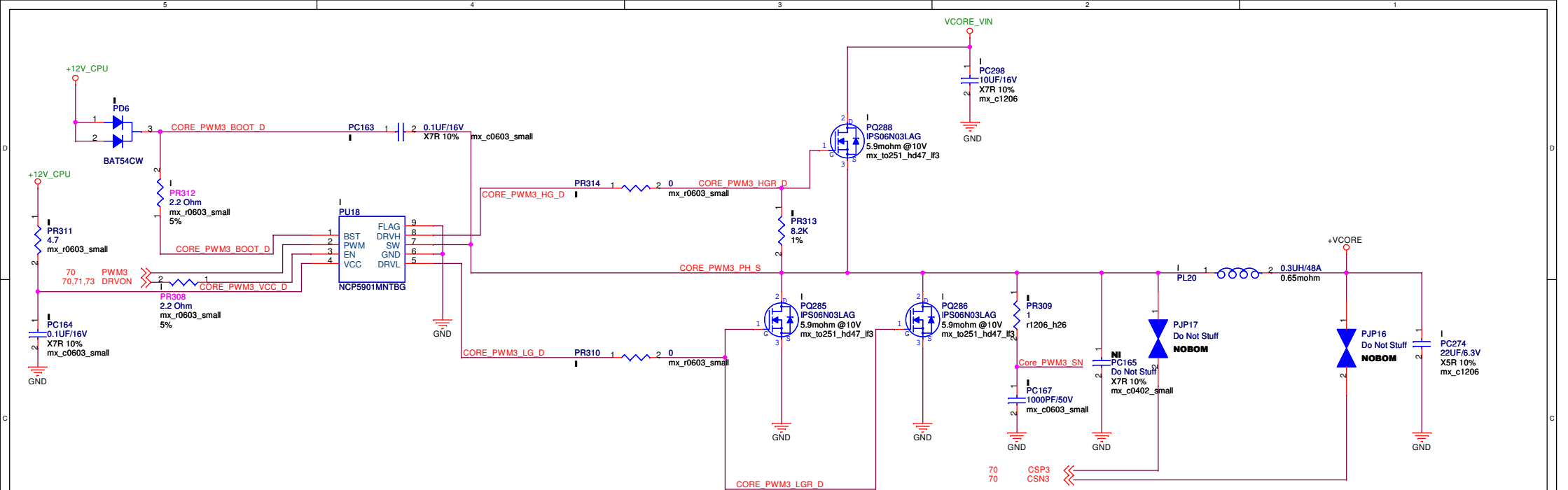
Pegatron Corp. Engineer: KJ Chang

Size A3 Project Name IPX61-DL Rev 1.00

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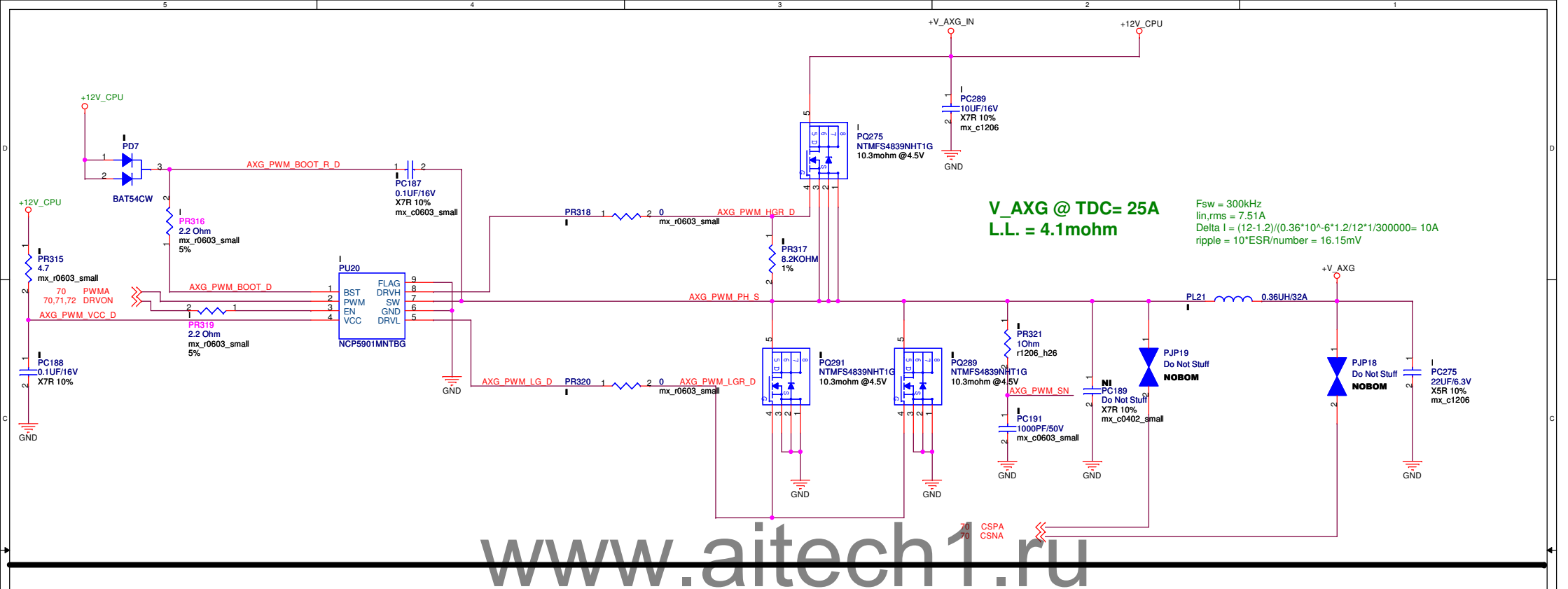


PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **VCORE DRIVER 2-2**

Pegatron Corp. Engineer: **KJ Chang**

Size	Project Name	Rev
A3	IPX61-DL	1.00
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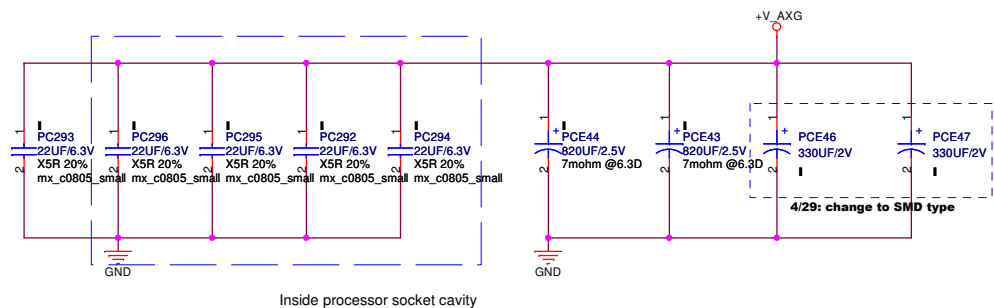


## Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP \*4  
 MLCC \*6



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **+V\_AXG DRIVER**

Pegatron Corp. Engineer: **KJ Chang**

Size Project Name

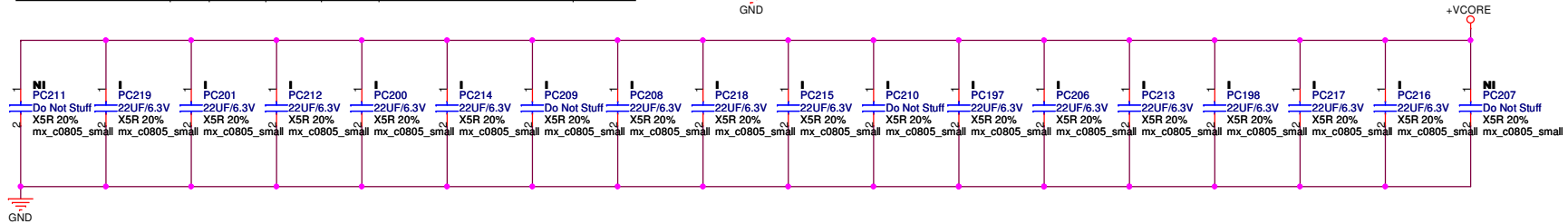
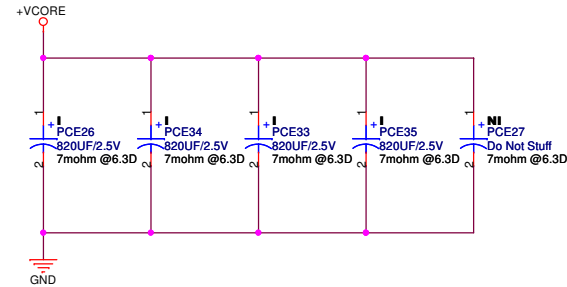
A3 **IPX61-DL** Rev 1.00

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# Output CAP

Table 30-2. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560μF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22μF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2, 3
Aluminum Electrolytic 390μF	4	51mΩ	6.1nH	Input		1
4.7μF X5R	9	7mΩ	0.6nH	Input		1



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PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : +V CORE O/P CAP

Pegatron Corp.

Engineer: KJ Chang

Size A3	Project Name IPX61-DL	Rev 1.00
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